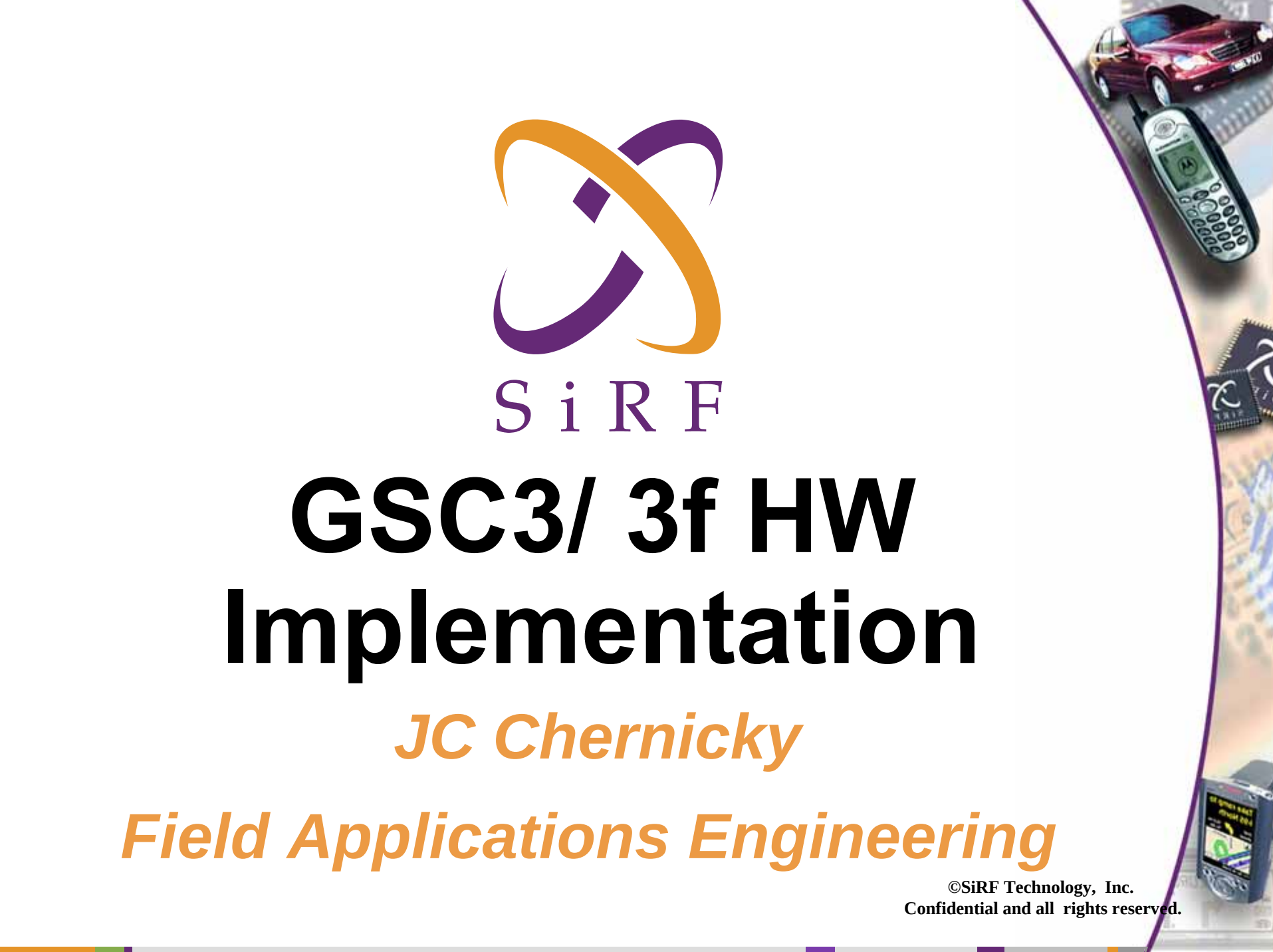


GSC3/ 3f HW Implementation

JC Chernicky

Field Applications Engineering

©SiRF Technology, Inc.
Confidential and all rights reserved.

Agenda

- **System on a Chip (SoC)**
  - Discussions and Block Diagrams
- **The New Package Approach**
- **The Signal Chain & Receiver**
  - Antenna Designs & Considerations
  - LNA and Front End Design Considerations
  - RF SAW Filtering
  - The GRF Chip
  - The TCXO
  - The GSP Chip and Configuration Considerations
  - Power Supply Concerns
  - Schematic & External Interfaces
- **Additional Comments and Considerations**

GSC3: The System on a Chip (SoC)

- The GSC3 is a new SoC product now available from SiRF.
- Contains the GSP3f baseband IC, the new low power SiGe GRF3i RF front end wirebonded side-by-side inside the package.
- Uses a new, GRF3i RF chip & has a low power Integer-n synthesizer approach.
- The GSC3f also includes a 4 Mb Flash wirebonded and stacked on the baseband die.

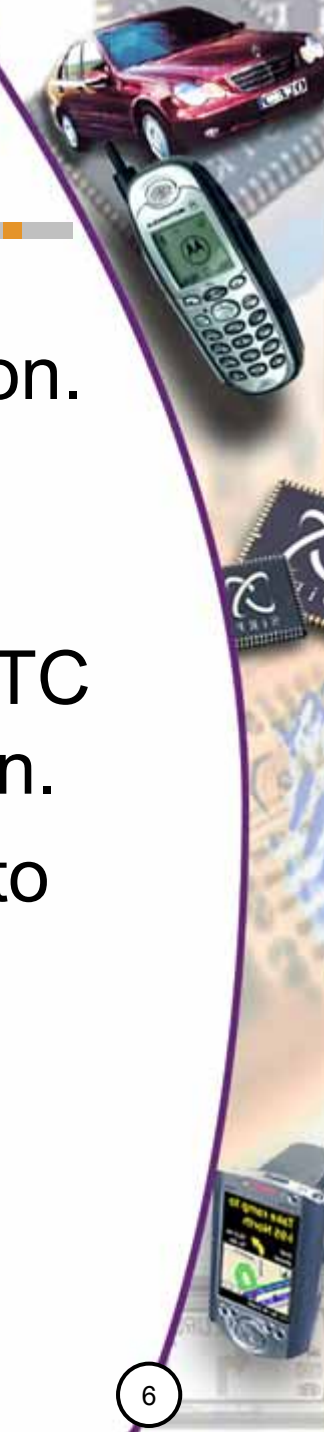
GSC3: The System on a Chip (SoC)

- Part Number: GSC3-7871, GSC3-7875 (Pb free), GSC3f-7877, GSC3f – 7879 (Pb free)
- Approximate Power - Peak: 80 mA (GSC3), Tracking: 60 mA (GSC3) @ 2.85 V.
- Chip-to-chip interface = CMOS. Routed outside of package.
- ESD=+/-2kV HBM all pins (Class 3). Exception: RFIN=+/-1.5kVHBM (Excellent)
- SW: GSW3.1 and SLC3.1 software will now run the older 3w3f design, and the new GSC3f design.

GSC3: The System on a Chip (SoC)

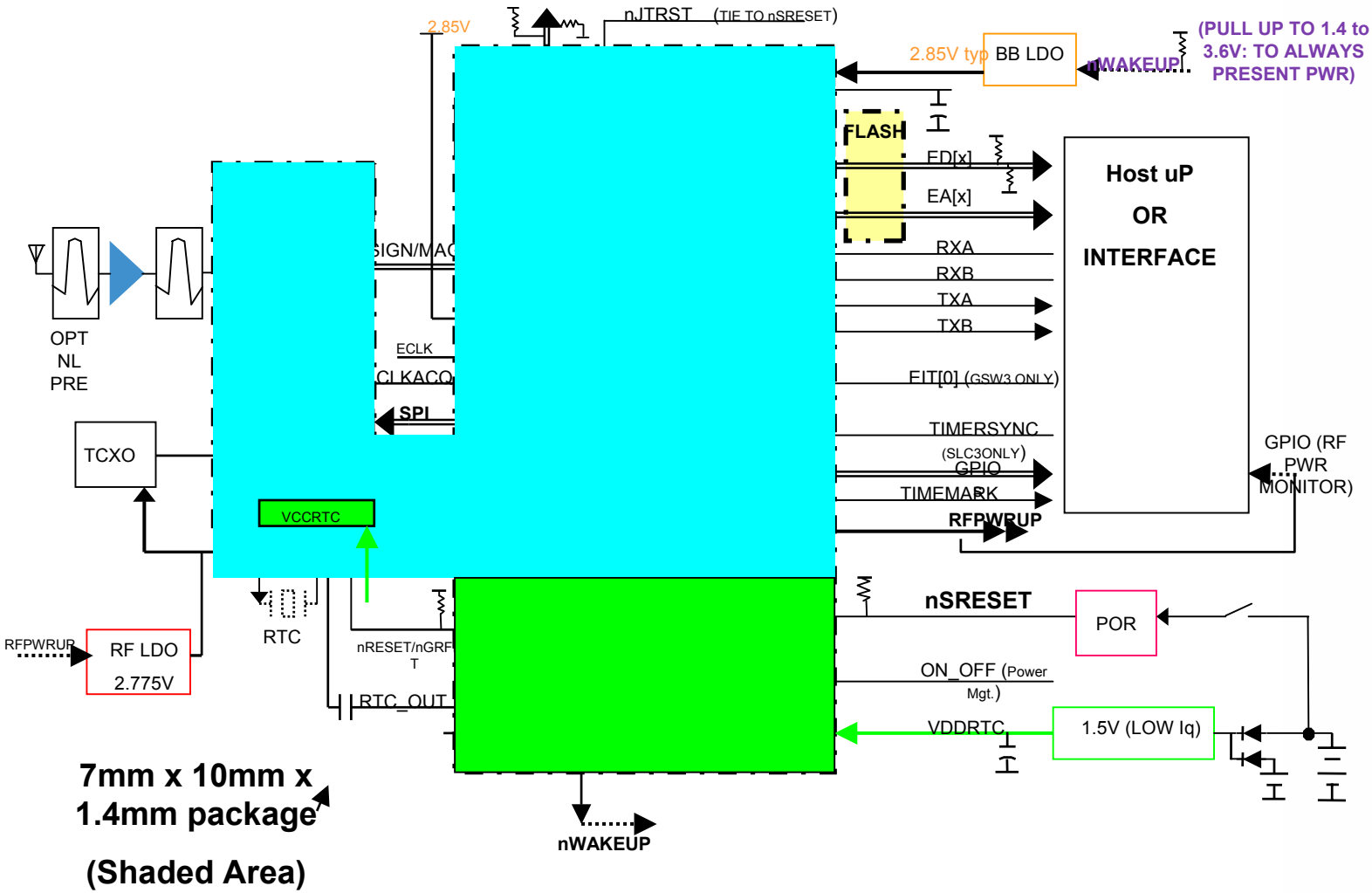
- Integer N PLL uses following references: 13, 16.369, 16.8, 19.2, 24.5535, 26, 33.6 MHz
- Clock interface (CLKACQ) from RF to baseband is now 16.369MHz during normal operation.
- Initial boot-clock could be a different frequency.
- RF to BB interface is CMOS. PECL no longer used.
- SPI interface into GRF3 allows the 3f ARM to program the Integer-N PLL.

GSC3 Continued

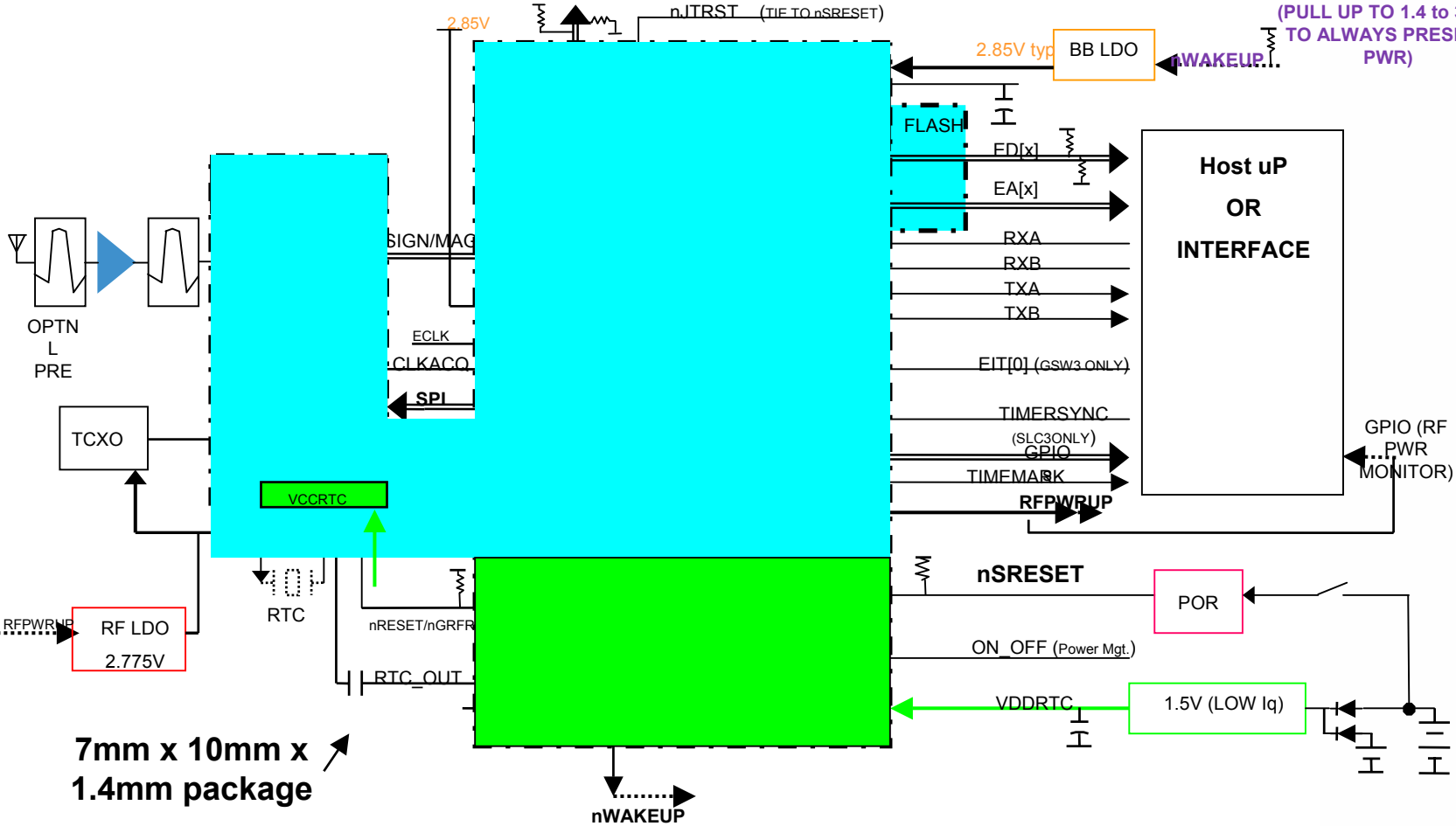


- Requires an *off-chip* LNA for proper operation.
- RTC oscillator cell internal to the RF chip in addition to the baseband chip.
- Reference design only populates RF chip RTC input which then feeds the baseband RIN pin.
- System Equivalent Noise ~ 4 dB (RF input to the correlators with 1 dB NF LNA)

GSC3 Block Diagram



GSC3f Block Diagram (with Internal Flash)



The New Package Approach

- Size: (140 pin BGA 7mmx10mmx1.4mm)
- Ball pitch = 0.65mm

The Signal Chain and Receiver Considerations

Antenna Designs & Considerations 1

- The Antenna: Perhaps the **MOST** important element to consider for a successful GPS design!
- Best signal reception is achieved with the proper antenna integration and orientation into the final package!
- Requires extensive pre-planning with antenna suppliers to develop the best integrated solution and performance.

Antenna Designs & Considerations 2

- Remember…GPS is a DEEP SPACE receiver, requiring the best conditions possible to amplify the incredibly weak GPS satellite signals.
- Optimizing the antenna in its final housing may take several iterations to achieve the needed results.
- Allow for ‘Plan A’ and a backup ‘Plan B’ for antenna development!

Antenna Designs & Considerations 3

- Use of combination antennas: NOT recommended!
- Extremely poor GPS reception will occur, unless antenna designer optimizes for GPS reception as primary function.
- Combination antennas also require some type of diplexer, which adds ~2-3 dB additional loss to the system NF.

Antenna Designs & Considerations 4

- Discussion of mismatch loss effects
- Discussion of ideal ground plane effects
- Discussion of ideal gain contours and radiation patterns

Antenna Considerations: Linear Antenna Concerns

1. Immediate 3 dB of loss relative to a circularly polarized (CP) antenna.
2. Spherical gain response instead of a hemispherical gain response. Will aggravate the multipath behavior & create poor position accuracy!! (lucky to achieve 50 m accuracy in some situations)
3. Poor LHCP relative to RHCP response.
4. Can have multiple gain nulls & average gain is MUCH lower than a good patch (-9 dB)

Antenna Suppliers and Options: Linear Polarization

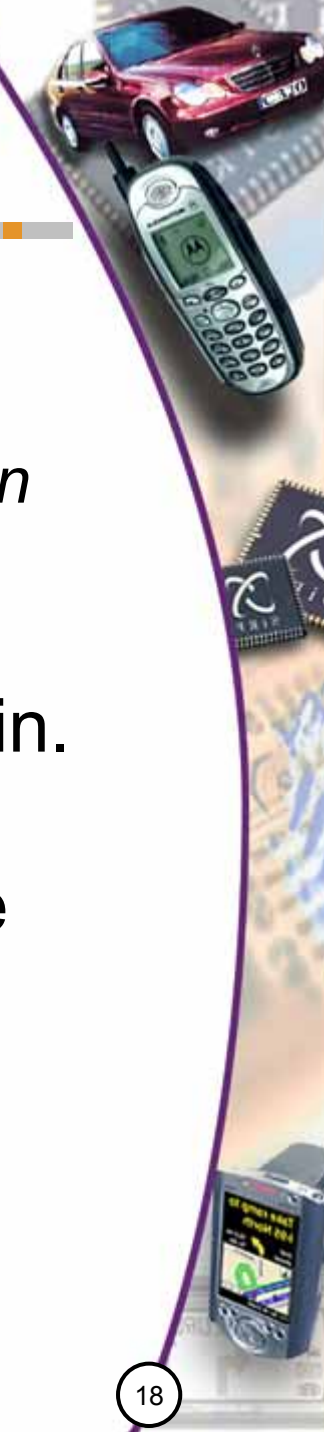
1. Filtronic - new (England)
2. FDK DA-5T26-new (Japan)
3. FRACTAL (New)
4. Kyocera GPS and GPS+BT (Japan)
5. Murata (Japan)
6. Taiyo-Yuden-new (Japan)
7. Others like Tyco or custom designs

Antenna Suppliers: Patch Elements

- FDK
- Kyocera
- Murata
- KDI (Korea)
- Many others

LNA and Front End Design Considerations

- LNA gain should be between 12 dB and 26 dB (assumes a patch antenna).
  - *This assumes the patch used has >3 dBic of gain*
- Linear antenna implementation should consider a minimum of ~14.5 dB of LNA gain.
- Excessive LNA gain (>27 dB) can introduce jamming spurs, degrade 3IP, and saturate the receiver. DO NOT EXCEED 27dB.

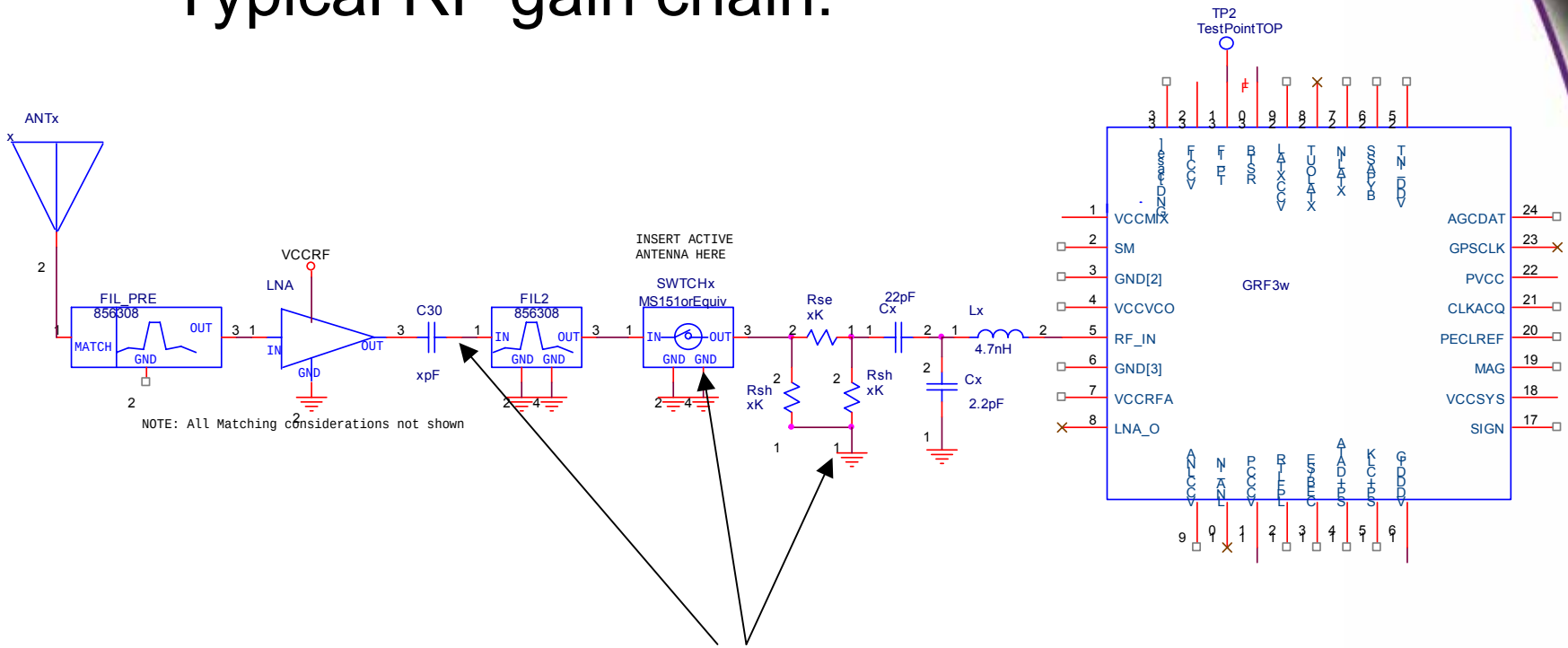


LNA and Front End Design Considerations

- LNA's have many tradeoffs to consider
  - Good NF vs. input AND output matching
  - Better match is preferred to enhance filter response – NF can degrade to 1.6 dB
  - Gain characteristics
  - High reverse isolation (minimizes filter interaction)
  - Broadband stability (out to 10+ GHz)

LNA and Front End Design Considerations

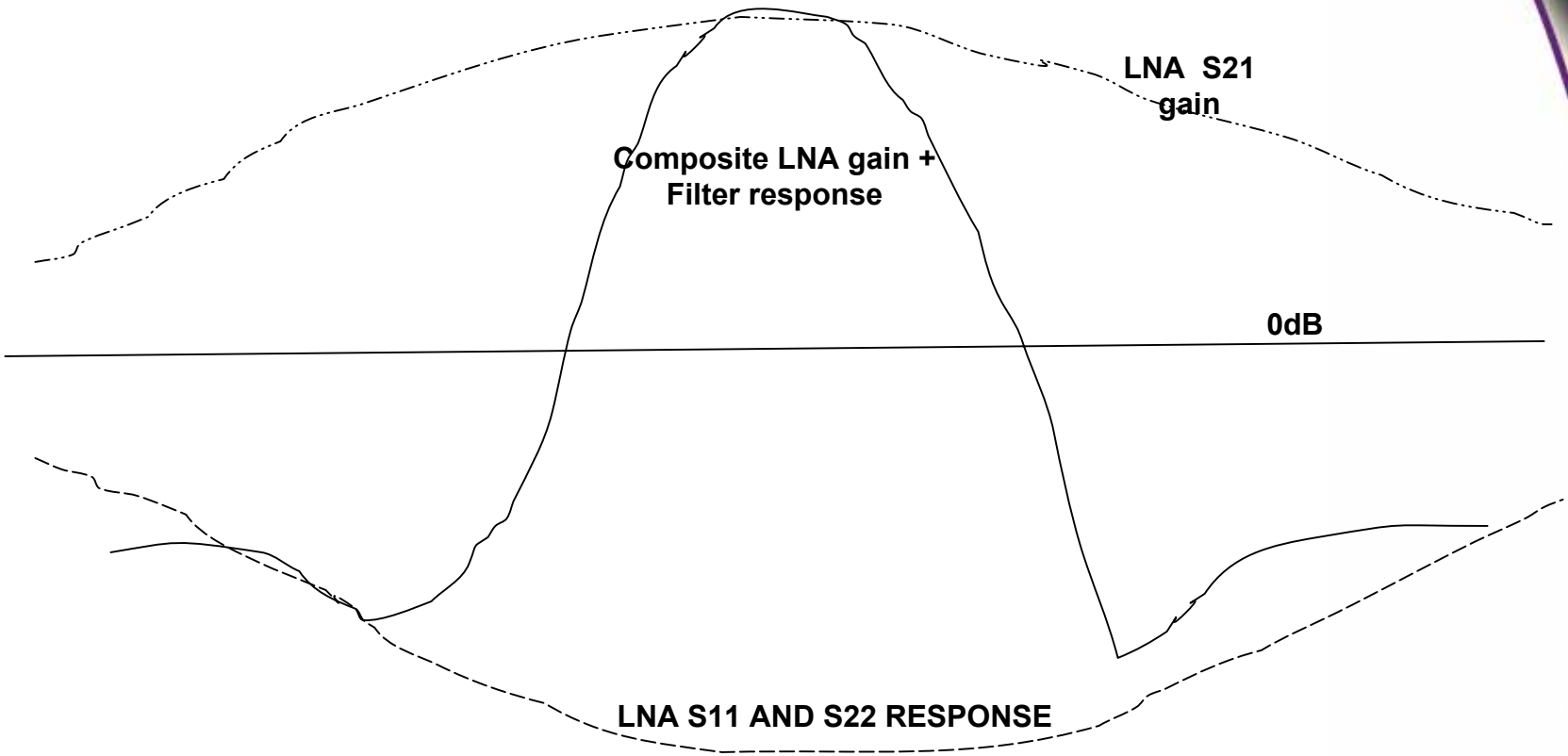
Typical RF gain chain:



Possible external connector/switch and isolation pad locations

LNA and Front End Design Considerations

Ideal LNA characteristics:



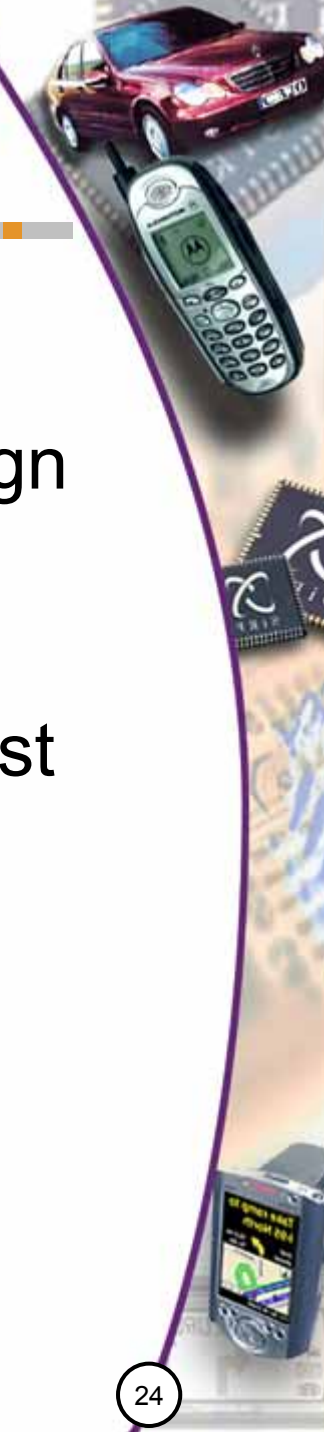
LNA and Front End Design Considerations

- Latest LNA's available with shaped gain response capabilities:
- Infineon BGA615L7 (new w/ shutdown)
- Infineon BGA 428 w/o shutdown
- NEC uPC8211 w/ shutdown
- ATMEL ATR0610 w/o shutdown
- JRC NJG1107 w/o shutdown

LNA and Front End Design Considerations

	1575 (+/-25 MHz)	1575 (+/-250 MHz)	1575 (+/-500 MHz)	
S21	~17 to 19 dB	~12 to 15 dB	~8 to 12 dB	
S11/S22	~16 dB	~6 dB	~3 dB (S22 improved with resistive pad)	
S12	~34+ dB		TBD	
NF	1.3 to 1.6 dB	N/A	N/A	
3IPo	>8 dB			Customer dependent on Icc demands

RF SAW Filtering



- In highly integrated environments rich with potential interference , SiRF suggests design implementations with PRE and POST LNA filters.
- Typically SAW designs are used for smallest size and low cost.
- Require *careful* matching and appropriate development efforts.

RF SAW Filtering

- PRE FILTERS rarely achieve < 0.7 dB IL
- Smaller size SAW filters usually imply lower ESD HBM ratings (50 to 200 V)
- Lucky to achieve 22 dB of rejection with some designs. Higher IL = Higher NF, and allows for slightly higher rejection levels.
- Still sensitive to matching for best filter flatness and rejection.
- Lowest loss designs from SAWTEK, EPCOS, Kyocera

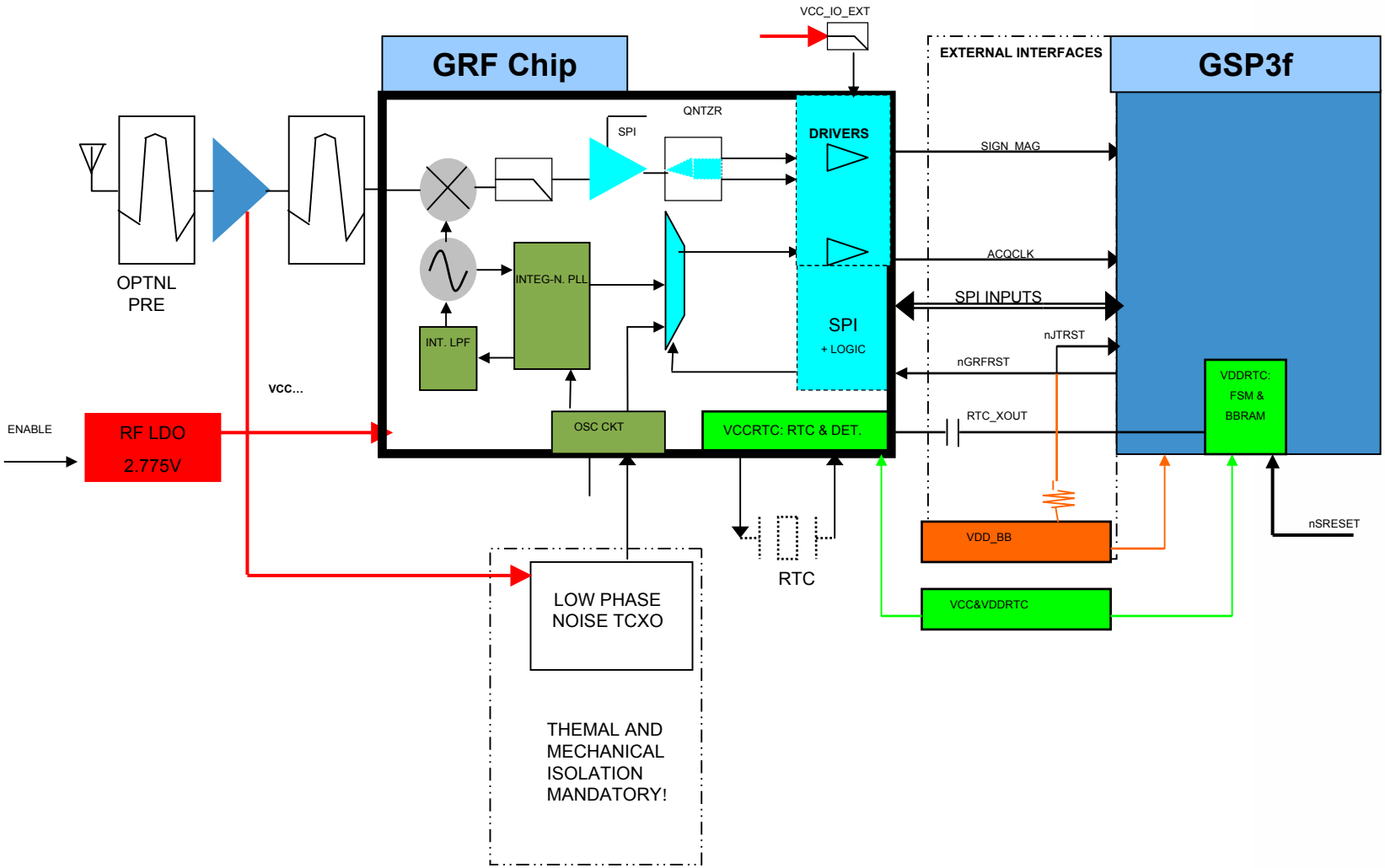
RF SAW Filtering

- **POST FILTERS** (Usually a SAW)

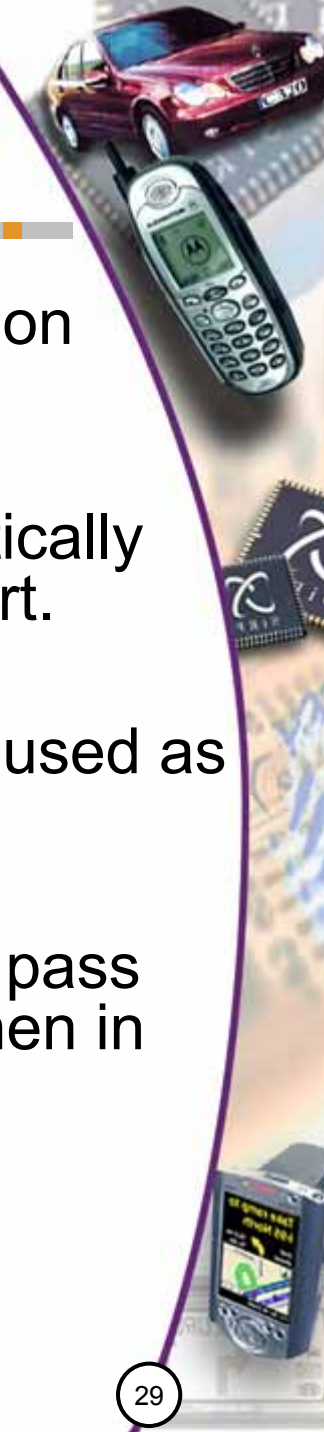
- Offer higher levels of rejection but requires tradeoff of higher IL.
- Usually not a problem because LNA gain sets NF.
- Still sensitive to matching for best filter flatness and rejection. Add -2 dB pad on output of post filter for improved broadband RL and filter matching (as space allows).
- Must characterize over temperature and production!!! Customers must implement mandatory internal RF analysis of their final layouts!

The GRF Chip

GRF Chip Block Diagram



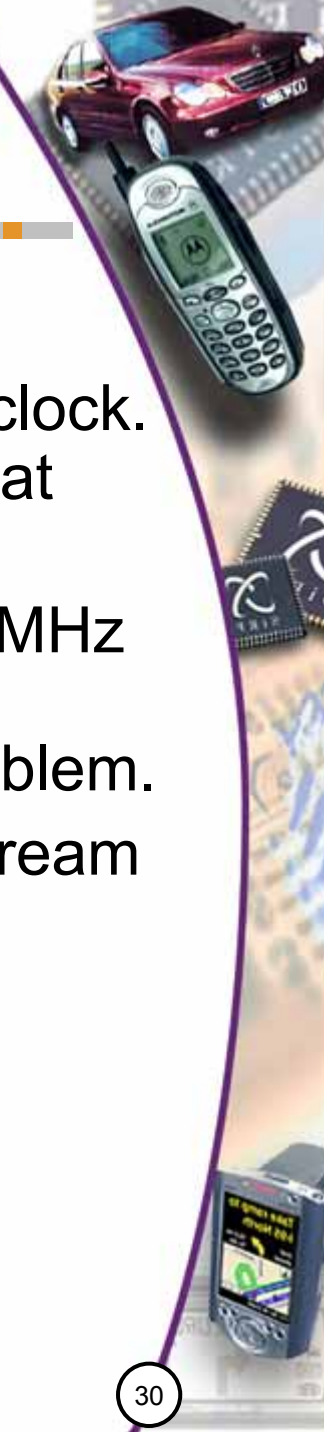
GRF Chip Details



- Integer-N synthesizer allows for lowest power operation (typically 14 mA with all sections on.)
- Works with 7 different frequencies. Software automatically compensates for incurred offsets with BBRAM support.
- Lowest power operation occurs when 16.369 MHz is used as TCXO reference (~10 mA).
- Why? Synthesizer can be disabled in this mode, and pass the TCXO directly to the baseband, saving ~4 mA when in full-power or CPU-only state.

GRF Chip Details

- The reference TCXO clock now becomes the boot clock. No need for concern with slow start up RTC clocks at initial boot up.
- Higher frequency references like 26 MHz and 33.6 MHz not fully tested for timing race conditions over temperature. We anticipate this should not be a problem.
- SPI controls the IF AGC levels. SIGN_MAG data stream is briefly ‘parked’ when AGC adjusts.



The GRF Chip Pins

VCC_IO_EXT

- Very noisy source due to CMOS edges. Decouple from RF supply with choke or LP Filter.

nRESET (Sometimes called RFRESET or nRSTB)

- Pull to VDD_BB supply with 1MΩ pullup. (**NOTICE**: THIS IS A CHANGE FROM THE PREVIOUS REF DESIGN)

SPECIAL RTC OSC AND DETECT CKT

- VCCRTC cell on GRF3 is fully isolated from rest of chip. Run at 1.5 V. Bypass with 2.2 µF.
- Same 2.2 µF bypass cap can be used for VCCRTC and VDDRTC. **DO NOT USE LESS THAN 2.2 µF.**
- Detect circuit sends error flag to GSP via SPI port if RTC clock is lost or miscount occurs.
- Couple to 3f RIN pin via 1000 pF series cap. Customers to verify waveform is always adequate after layout.

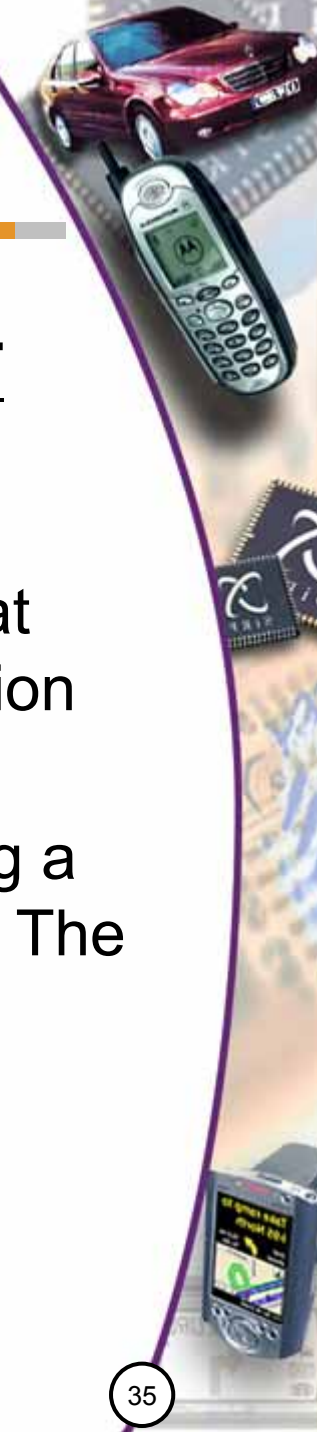
The TCXO

TCXO Recommendations

- ***Extremely Critical Component!***
- SW is set up for a 0.5 ppm temperature-rated TCXO
- Drive of 200 mV_{PP} to 1200 mV_{PP} AC coupled input
- Extremely Stable RF power supply required
  - No transients should be present
  - Lowest-noise regulator possible, PSRR > 65 dB @ ~100 Hz
  - Low temperature dependence (< 1.5 mV/ºC)

- Suppliers to consider:
  - **Proven Supplier:** Rakon (e.g., model TX2142)
  - Alternates to consider: CMAC, Kyocera (NEW), Toyocom, TEW

TCXO Details



- Next to the antenna, the **TCXO is THE next MOST important BOM part.**
- We advise all customers that the best success for specified weak signal acquisition will be TCXOs that meet the requirements of the GPS Clock specification for the SiRFstarIII system dated July 2004 or later.
- Use of an inferior TCXO could be likened to running a high performance sport car….ON DIESEL FUEL!! The desired results will not occur in the vast majority of environments.

TCXO Details

- TCXOs need stable power supplies over temperature. Excessive changes in supply voltage over temperature will affect the frequency change, and increase the search times.
- Some of the newer TCXOs by Rakon and Kyocera have built in regulators, and are more immune to this problem.
- TCXOs MUST meet the necessary close-in phase noise, aging, temperature stability, G-sensitivity, and many other parameters for successful weak signal acquisition.

TCXO Details

- New TCXOs now available from Kyocera and Rakon with stellar performance characteristics!
- 3.2 x 2.5 mm 5th order TCXO compensation and new, improved 3rd order compensation.
- Built in regulators now available.
- Extremely reasonable cost/performance
- Newer designs in work approaching 2.5 x 2 mm in size, and lower power.
- Use of alternate sources requires **considerable** resources to validate performance.

Configuration Considerations

External configuration straps for supported Clock Reference Frequencies:

****Note that these configurations may be different than the GRF3w/GSP3f design.**

	Frequency Selector								Boot Clk	GRF3i	Boot
Boot-Clk Freq (MHz)	JTCK	JTDI	ED[13] (p/u)	ED[12]	ED[11] (p/u)	ED[10] (p/u)	ED[9] (p/u)	ED[7]	ED[3]	ED[2]	ED[1]	ED[0]
24.5535	0	1	x	x	x	x	x	0	1	1	1	0
13.0000	1	1	0	0	0	0	0	0	1	1	1	0
16.369	0	0	x	x	x	x	x	0	1	1	1	0
16.800	1	1	0	1	0	0	0	0	1	1	1	0
19.200	1	1	0	1	1	0	1	0	1	1	1	0
26.000	1	0	x	x	x	x	x	0	1	1	1	0
33.600	1	1	1	1	1	1	0	0	1	1	1	0

p/u = Internal pull up present

Use External Pull-up/down resistors to set the bits.

Configuration Considerations

The following Data Bus pins are read and latched at Reset

ED0 Read on power up to determine boot (1=internal, 0=external)

ED1 Select RF chip 0 = GRF3w selection, 1 = GSC3 RF

ED2/3 Read on power up to determine Boot Clock Source:

ED3	ED2	
0	0	= GSC RF Chip
0	1	= RTC Clock
1	0	= ECLK
1	1	= CLKACQ

ED7 Set bus width (0=16 bit, 1=Reserved)

The GSP3 Signal Processor

SPI BUS

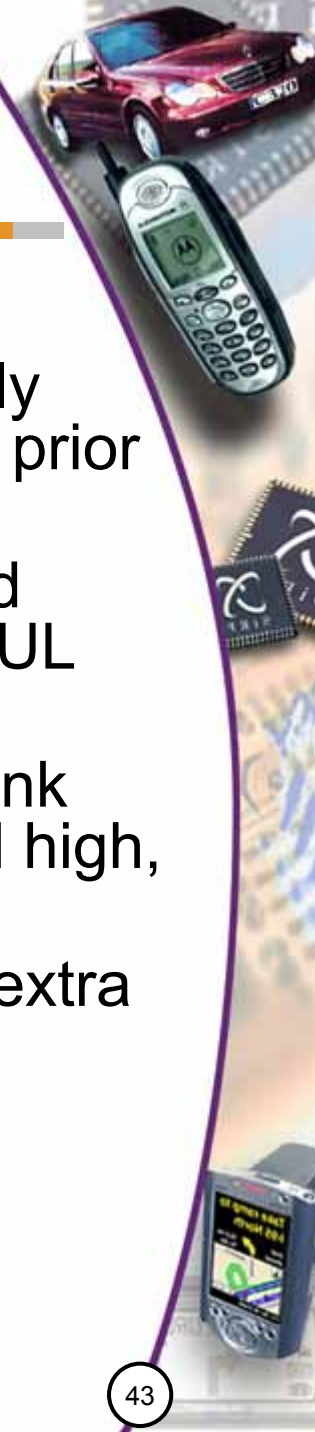
- The SPI bus on the GSP3f is a master only.
- Its key functionality is for configuring the RF chip upon each and every power up and during power management states.
- Also provides AGCDAT control for IF gain.
- It is not available for customer access.

ECLK

- CMOS clock correction signal INPUT for use with SLC3.x code.
- ± 0.5 ppm or less (± 0.1ppm absolute error preferred)
- Must be non-steered during clock correction, or
- MUST BE <5 ppb/900msec drift for 15 dB-Hz!
  (or ±2.5ppb/900ms w/SLC3.1 code)
- 13 MHz to 26 MHz input range allowed.
- Ideally should be a non-multiple integer of XTALIN freq (i.e. 1.14739, not 1.25 or 1.33).
- Very low jitter required (Exact value TBD)
- Has internal pull down. OK to float if not used.

GSP Chip Details

- To have hibernate current ~10 μA, you must properly isolate the RTC circuitry from the rest of the system prior to turning off core power.
- To do this, software sets bit 9 of the RTC Status and Control Register (the isolate bit) DURING GRACEFUL SHUTDOWN.
- If you **fail to allow** for proper graceful shutdown (yank power), and if a signal line is allowed to be asserted high, IDDRTC current may exceed 200 μA, or more!
- External inputs (ECLK, RXA, RXB, etc.) can cause extra current draw if active or high (discussed later).



EIT[0]

- Available for users – not used by SiRF.
- Can be made active high or active low under software control.
- No internal pull-up or pull-down resistor.
- Will not wake up a system in HIBERNATE state, only sleep state (core power still present).
- See software training for usage details.

ON_off

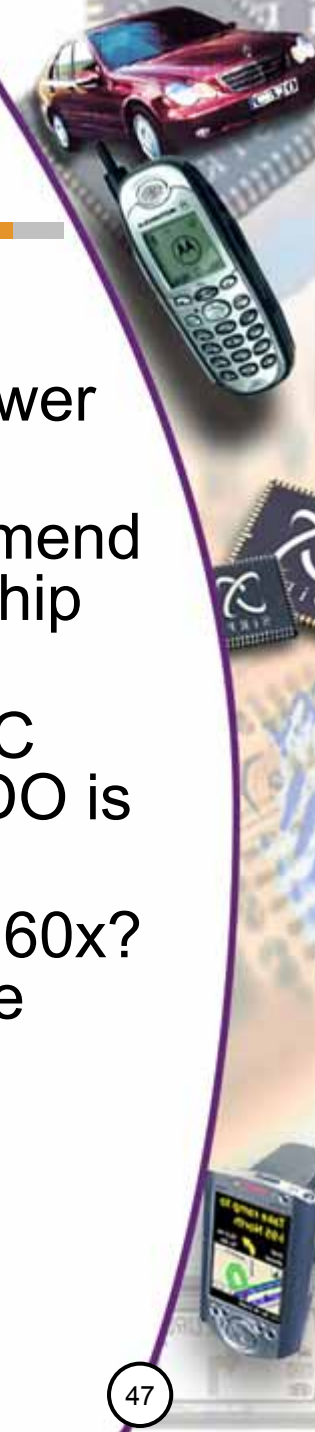
- Rising edge triggered.
- This pin was intended to turn the receiver ON or OFF, but during the design process, OFF was disabled for certain reasons.
- This pin should be pulled low with a 4.7 kΩ resistor and shunt (TBD) cap for noise reduction.
- This is dependent on the drive capability of the external driver.
- Min/Max rise times still TBD. Keep noise to a MINIMUM!

ON_off

- **ON_off** is a DIRECT hardware connection to the internal state machine. Activation of this pin will wake up the receiver from a sleep or stand-by state, such as in a push-to-fix application.
- **ON_off** should NEVER be activated when the chip is in a power-on state – it will advance the state machine (may change in later chips versions;TBD).
- Monitor power from an external host before activating **ON_off** MUST be implemented.

nWAKEUP

- Pull-up to an ALWAYS-PRESENT, non-switched power source.
- Do not pull higher than 3.6 V, thus we do not recommend pulling it up to an unregulated supply (could cause chip failure).
- SiRF suggests pulling up **nWAKEUP** to the VDDRTC output regulator as an alternate, providing the BB LDO is properly chosen w/ adequate enable thresholds.
- **nWAKEUP** can enable a Torex XC6401, a Ricoh 1160x? series of regulators (or similar, with active low enable signal).
- Baseband LDO active LOW, RF LDO active HIGH.



TIMERSYNC

- Used to set a timestamp for SLC3.x time aiding information.
- Also noted as GPIO[15]/nCS[3]
- Rising edge triggered CMOS input.
- Must be >123 ns wide minimum
- Should be ~1 ms max.

THE RTC Section

- Crystal Frequency: 32.768 kHz ± 20 ppm
- Frequency drift at 25° C: -0.4 ppm/ $^{o}C^{2}$
- ROUT Output Voltage: 1.2-1.5 V_{PP}
- Optional External RIN Input Voltage
  - Minimum 0 to 0.3 V CMOS level
  - Maximum 1.2 to 1.6 V CMOS level
- RTC Time = GPS Time ± 25 µs, verified every second
- Rise/Fall times 2 to 8 µs, jitter should not be noticeable.
- VDDRTC Power-up Ramp Up Time < 10 ms

Battery Backup and BBRAM

(**THE KEY** to successful Hot starts)

- BBRAM holds all the critical information needed to optimize hot starts, and therefore keep battery drain to a minimum.
- Failure to provide for proper BBRAM and backup will extend TTFFs and increase current drain.
- Discuss safety shutoff circuits for low capacity coin cells: OEM responsibility.

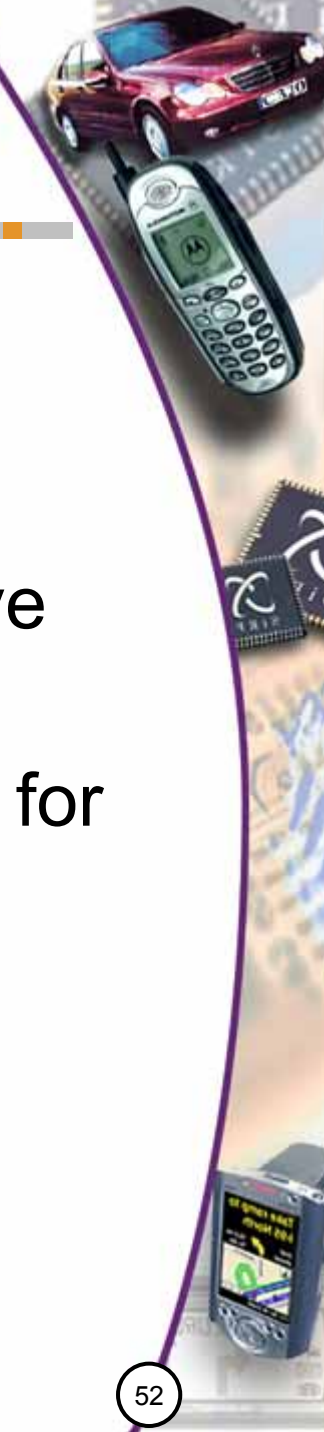
GSC3 Power Supply Limits

Core	VDDk	1.50 V nominal (1.40 V - 1.60 V)
I/O	VDDI/O	2.85 V nominal (2.70 V - 3.60 V)
Flash	VDDF	2.85 V nominal (2.70 V - 3.60 V)
RF	VCCRF	2.85 V nominal (2.70 V - 3.15 V)
RTC-RF	VCCRTC	1.50 V nominal (1.40 V - 1.60 V)
RTC-BB	VDDRTC	1.50 V nominal (1.40 V - 1.60 V)

NOTES:

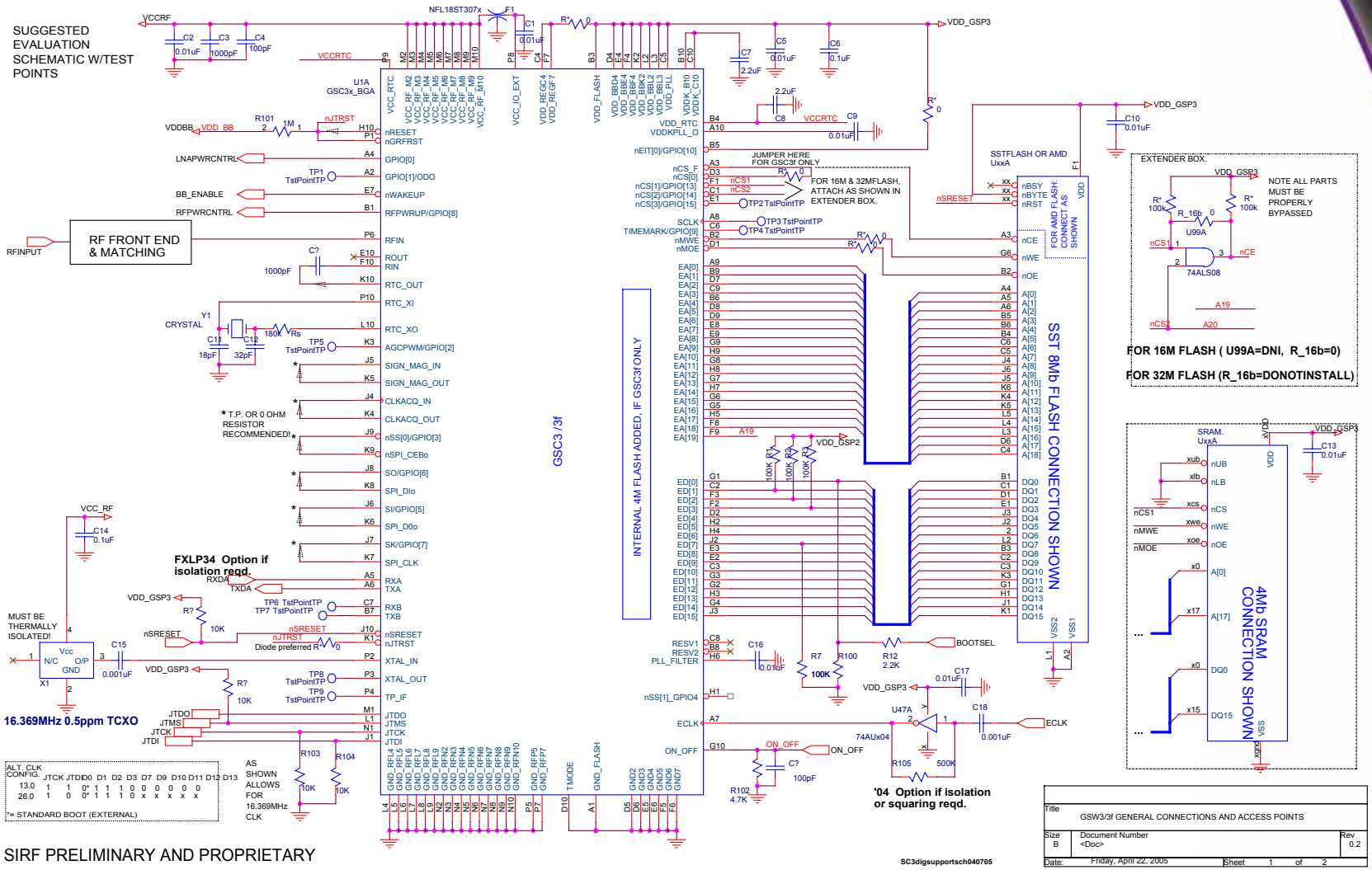
1. **VDDBB power supplies VDDk, VDDI/O, and VDDPLL regulators.**
2. **Do NOT allow supply to exceed 3.0 V when integrated with GRF3 RF chip**

Power Supply Concerns



- New *DUAL* CSP regulators available from Torex, and Seiko.
- Can be ordered with active high, and active low enable pins.
- External 1.5 V LDO for VDDRTC. Choose for low Iq. Diode ‘OR’ primary and backup battery to this LDO input.

Simplified Schematic



SIRF PRELIMINARY AND PROPRIETARY

Title	GSW3/3f GENERAL CONNECTIONS AND ACCESS POINTS	
Size B	Document Number <Doc>	Rev 0.2
Date: Friday, April 22, 2005	Sheet 1 of 2	

Additional Comments and Considerations

- JTAG
  - Pull JTRST high with 10 kΩ! (NEW schematic mod!)
  - JTDO can float.
  - JTMS pull high with 10k.
  - JTDI, JTCK determine boot clocks.
- GPIO monitoring of VDD_BB and VCC_RF.
  - Needed to ensure 99.9999 % successful operation of ON_off (still characterizing).

External Interfaces

- RX Lines and TX lines may need a dual supply isolation buffer like an FXLP34 to avoid CMOS high states while in Hibernate.
- ECLK: If signal squaring is needed, consider a SINGLE stage device such as a TC7S04 in active bias configuration.

External Interfaces

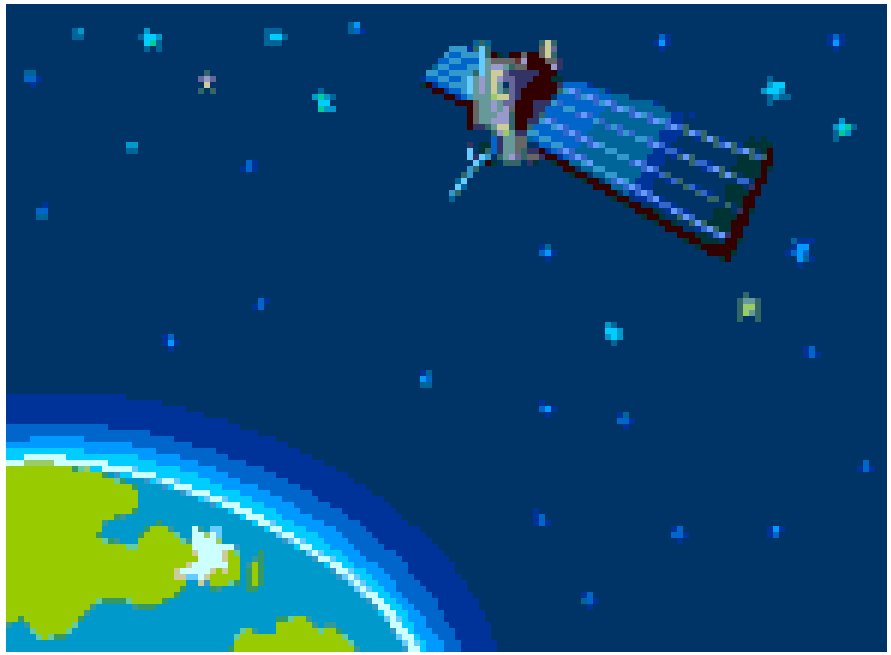
- Verify the chosen ECLK buffer can be driven safely with power off to avoid excessive leakage current while in HIBERNATE, if ECLK cannot be disabled.
- GPIOs (Timersync, nCS, etc)…Make sure these lines are held low during Hibernate.

External Interfaces

Test Points

- Mandatory
  - **TPIF, nCS_F (or 0 Ω resistor), SCLK, CLKACQ, SIGN_MAG, RTC XTAL_OUT, SPI_CLK, SPI_DI, SPI_CEB**
- Recommended if space permits
  - **EA0, nCS3, ECLK, TXB, RXB, ROUT, AGCPWM**

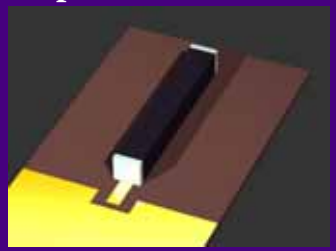
Questions?



Technology Overview: Antenna Technology (1.575GHz T-Y Chip Antenna Example)

E911 / GPS

Shapes



11.0x1.6x1.6 mm

Ceramic Dielectric Material

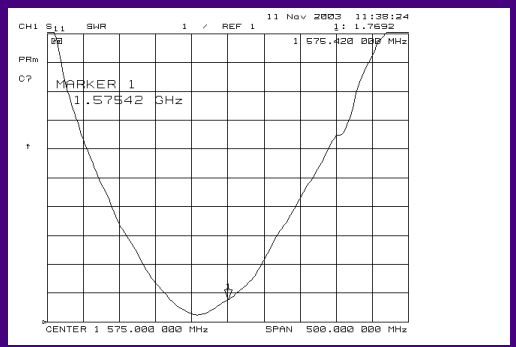
Ag Metal

Electrical Characteristics

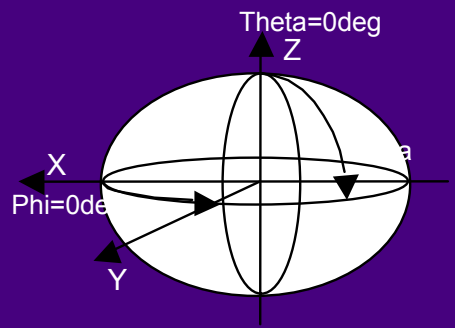
@ 1.545 GHz	Phi:0cut	Phi:90cut	Theta:90cut
Gain(dBi):Phi	-28.7	0.6	-2.7
Gain(dBi):Theta	-2.4	-13.7	-11.8

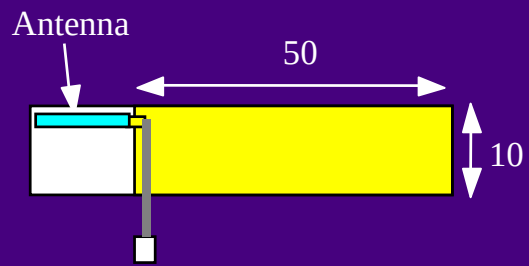
Efficiency : -1.1dB

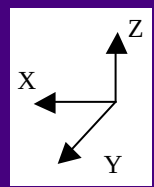
VSWR Characteristics



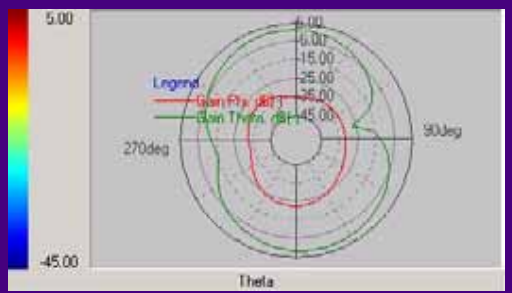
GND Size : 50 x 10 mm







Radiation Pattern



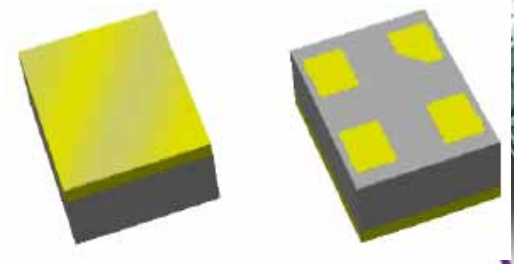
Phi : 0 [deg] cut

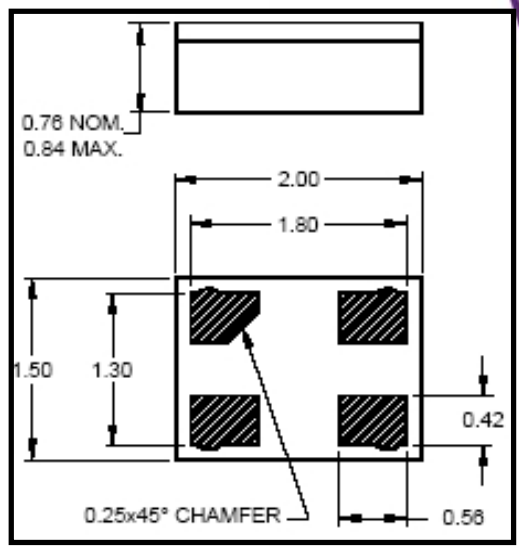
Phi : 90 [deg] cut

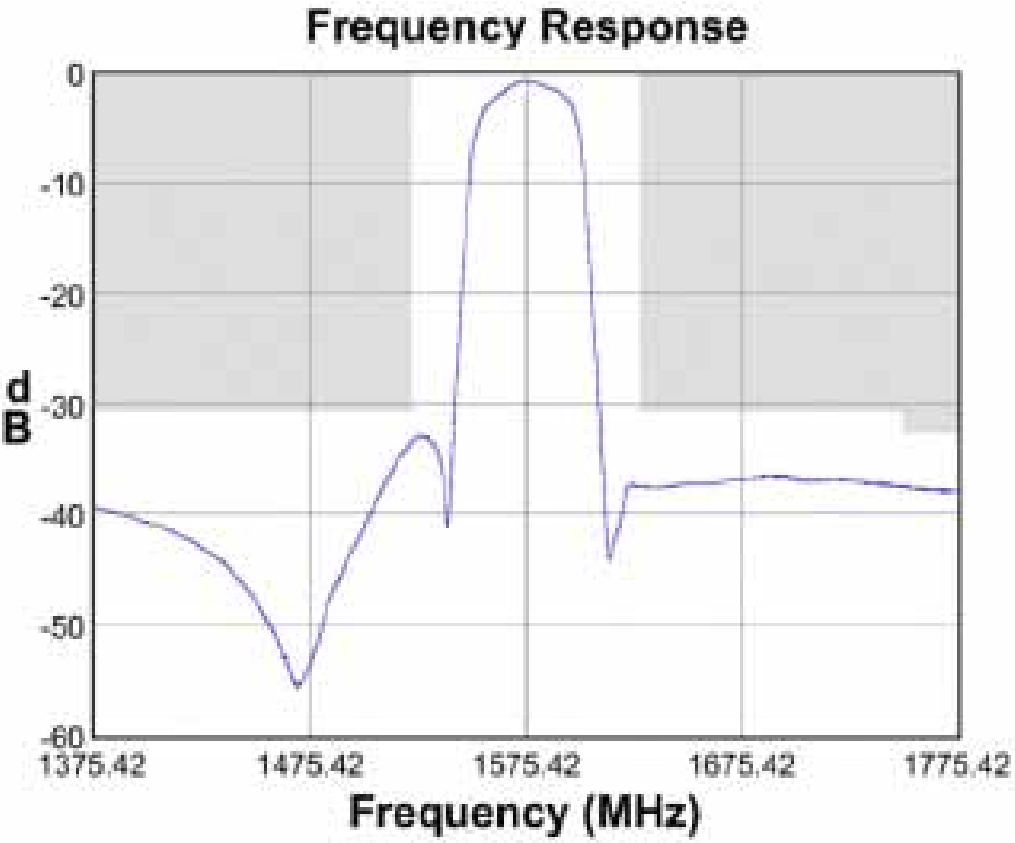
Theta : 90 [deg] cut

2 x 1.5 mm, High rejection Example – P/N 856308

- For GPS applications
- Compatible with SiRF Star III
- No impedance matching required for operation at 50 Ω
- Single-ended operation
- Chip Scale Package (CSP)







SPEC	PERFORMANCE
IL (dB)	1.0 Typ
Pssbnd var (dB p-p)	0.25 Typ
I/O Return loss (dB)	18 Typ
Temp range	-40 to +85 癈