SiRF Application Note: SiRFstarIII GPIO Usage

Document Number : **APNT3005**
Revision 1.0
4/4/05

Author: Carl Carter

Table of Contents

1. INTRODUCTION

Customers who wish to use the SiRFstarIII chipset as the primary processor in their design usually need to monitor or control external devices as well as the GPS receiver. General Purpose Input/Output (GPIO) pins are provided for that purpose. In this document we will introduce the available GPIO pins, and describe how to control them.

1.1. Background

SiRFstarIII baseband chips (GSP3*x* devices) contain varying numbers of GPIO pins usable by customers. Some of the pins have secondary functions which may preclude their use as a GPIO in some implementations. This document explains the alternate functions, how to control the pin assignment, and how to utilize the GPIO functions of those pins selected for use by the system designer. Section 3 below presents a review of the available GPIOs, their alternate functions, and available software resources to use them. Section 4 provides some recommendations on selecting a GPIO for a specific design. Appendix A contains a chart summarizing the hardware interfaces to all of the GPIO lines.

In addition to the GSP3*x* devices, SiRF also offers single-chip solutions based on the SiRFstarIII chipset. These chips, designated GSC3*x*, have similar GPIO assets as the GSP3 devices, and are also covered in this document.

2. APPLICABLE DOCUMENTS

SiRFstarIII SDK User's Manual

3. GPIO Pin Usage

3.1. Alternate Functions

Several of the GPIO pins have assigned functions that may make them unavailable for use as a GPIO. Table 3-1 lists the GPIO pins and their alternate functions, and indicates specific software builds which may make use of that function.

Table 3-1: GPIO Pin Alternate Functions

GPIO Pin Number	Alternate Function	Software Using Alternate Function
0	Power Control	All versions using power management
1	Odometer input	SiRFDRive only
2	AGC Pulse to RF	All using GRF3w RF chips
3	SPI Slave Select[0]*	All using GRF3 RF chips
4	SPI Slave Select[1]/MAG	None
5	SPI SI*	All using GRF3 RF chips
6	SPI SO*	All using GRF3 RF chips
7	SPI SK*	All using GRF3 RF chips
8	RF Power Control	All versions using power management
9	Timemark	Any using 1 PPS (typically GSW3)
10	EIT[0]	User-defined external interrupt
11	Not present	
12	Not present	
13	Chip select 1/nCTS	Any using UART hardware flow control
14	Chip select 2/nRTS	Any using UART hardware flow control
15	Chip select 3/YCLK	None

* For the GSC3*x* chips, those pins marked with an asterisk are dedicated to their alternate functions and cannot be used as GPIOs. Other pins not marked may be used as a GPIO unless specific software versions require use of the alternate function.

Selecting an alternate or GPIO function is done by use of the GPIO Select registers (address 0x80100100 and 0x80100104). Pins that are to be used as GPIOs should have a 0 in the corresponding bit of the GPIO Select register, while those where the alternate function is to be used have a 1 in the corresponding bit. Table 3-2 lists the bits of the GPIO Select register and the GPIO pins which they control. An exception to this is when pins have two alternate functions (indicated by two functions separated by a / in Table 3-1, specifically, GPIOs 4, 13, 14 and 15). In that case, the first alternate function listed is controlled by the GPIO Select register while the second function listed is controlled by bit 13 of the associated GPIO State register. See section 3.2.

Table 3-2: GPIO Select Register Bit Functions

Bit	Function	GPIO Pins Controlled
0 (LSB)	Odometer input	1
1	AGC Pulse to RF chip	2
2	SPI Bus Slave Select [0]	3
3	SPI Bus Slave Select [1]	4
4	SPI Bus SI, SO, SK	5-7
5	RF Power Control	8
6	Timemark	9
7	EIT[0]	10
8-9	(Reserved)	
10	Chip select 1	13
11	Chip select 2	14
12	Chip select 3	15
13-31	(Reserved)	

Note: A 1 in a bit sets the corresponding pin[s] to the alternate function; a 0 in a bit disables the corresponding alternate function and permits the pin[s] to be used as a GPIO or a secondary alternate function (see section 3.2).

3.2. Secondary Alternate Functions

SiRFstarIII has four GPIO pins that perform a second alternate function. To activate this function, the pin must be set as a GPIO in the GPIO Select register, and to a specified input or output setting (depending on the specific pin). Then bit 13 in the GPIO state register that controls the GPIO is set to one to designate the secondary alternate function. Table 3-3 lists the secondary alternate functions and the required direction of the GPIO. The register controlling the secondary function is also listed.

Table 3-3. Secondary Alternate Functions

GPIO	Secondary Function	Controlling Register	GPIO Setting
4	Magnitude from RF	GPIO_State0	Input
13	nCTS for UART A	GPIO_State2	Input
14	nRTS for UART A	GPIO_State7	Output
15	YCLK	GPIO_State8	Input

The Magnitude function for GPIO 4 is used with the GRF2m/GRF3w RFIC, which has a two-wire data stream. Other GRF3 RFICs use a single-wire data stream and multiplex the Sign and Magnitude data onto the same wire. The nCTS and nRTS functions of GPIO 13 and GPIO 14 are hardware flow control lines for UART A. nCTS is an input which designates that the UART connected to the other end of the serial line is ready to accept characters ("Clear To Send"); nRTS is an output from

UART A indicating that it has data to send ("Request To Send"). YCLK is an input required when the receiver uses a CDXO clock source.

3.3. GPIO Pin Access Functions

Several software routines are available to assist in accessing the GPIO pins. These routines are documented in file MISC_sif.h, with supporting documentation and helpful definitions in file GPIO.H. The functions available include functions that set and clear the alternate functions, functions to set the direction of a GPIO, and functions to read from and write to the pins.

In addition to the above functions, there are some routines that permit coordinated usage of the GPIOs. These functions permit reserving GPIOs, unreserving them, and determining if they are currently reserved. Using this mechanism, various pins can be given multiple functions without the user software interfering with the GPS software. A specific example of this capability would be sharing the SPI bus by use of the Slave Select pins. Some SiRF RF chips use the SPI bus to program their functions. By designating one Slave Select pin for the RF chip and the other for a user's chip, both the user software and the GPS software can share use of the bus without interfering with each other.

4. SUGGESTED GPIO USAGE

Which GPIO you select for a specific application should be guided by your overall system design. Some GPIO pins are required for functions that may or may not be used in your design. When planning your system design, be sure to consider not only the planned design, but future modifications and versions which may utilize other features. When a selected GPIO must be changed, not only does the hardware change, but the software interface also must be considered. Careful selection of GPIO lines up front may make the maintenance of user-developed software reusable in future designs.

4.1. RF Chip Interface

A review of the SiRFstarIII RFIC data sheets shows that there are different interface formats in use depending on which RFIC you select. Considerations for each are shown in the paragraphs that follow.

4.1.1. GRF3i RFIC Interface

The GRF3i RFIC uses a SPI interface to control the chip. In addition, it uses only 1 wire for the sampled RF data stream. The SPI interface requires a total of 4 wires: a chip select, clock, data in and data out. These functions use GPIOs 3, 5, 6 and 7, respectively. The use of a single-wire data interface for the RF

sample does not require any GPIO pins. This RFIC uses the SPI interface to control the AGC, and uses a 1 ms update rate. If you use the GRF3i RFIC, you cannot use the SPI interface for any other purpose. However, GPIO 4, SPI Bus Slave Select[1], is not used with this interface and can be used by customer software.

4.1.2. GRF3w RFIC Interface

The GRF3w RFIC uses a two-wire interface for the sampled RF data stream. For the second wire, GPIO 4 is used in its second alternate function. In addition, it uses a pulse-width modulated signal for AGC feedback from the baseband to the RFIC. For this function, GPIO 2 must be used. It uses the same SPI interface (GPIOs 3, 5, 6 and 7) as the GRF3i, but does not use it except during startup, and when changing power settings (such as when using power management). SiRF's use of the SPI bus for RFIC control, and the dedication of SPI interrupt handling to SiRF's drivers makes use of SPI functions not possible for customers. Therefore, GPIO 4 is available for customer use as a GPIO.

4.1.3. GSC3*x* Chips

The GSC3*x* chips dedicate GPIOs 3, 5, 6 and 7 to control the internal RFIC using SPI bus functions. The affected pins are not interconnected inside the GSC3 package and must be connected using external loopbacks. See the appropriate data sheet for the specific device you will be using. The GSC3*x* chips use a single-wire sign interface between the RFIC and baseband chips for sign and magnitude, so GPIO 4 is not used by the chip and may be used by customer designs. AGC feedback from baseband to RF section is also over the SPI bus, so GPIO 2 is available for customer use as well.

4.2. UART Hardware Handshake

A receiver that needs to use hardware handshake on serial port A must dedicate GPIOs 13 and 14 for that purpose. Historically, SiRF has not provided hardware handshake, so the requirements for this feature should be very low. Before implementing handshake, analyze the requirements carefully to ensure it is a true necessity.

4.3. Power Management

GPIO 8 is designed to perform part of the power management function of the receiver. It is generally the signal from the baseband chip to the RF section to turn on and off completely. Some receivers also implement a power-management scheme where portions of the RF section are turned

off to reduce power consumption under more limited conditions (what was called "CPU Only" mode in SiRFstarII receivers). For that purpose, GPIO 0 is typically used in the SiRFstarIII software. Note that this is not a designated alternate function controlled by the GPIO Select register, or a secondary alternate function controlled by the state register. It is simply a designated use of a GPIO register controlled by the software.

4.4. Extended Memory

A receiver that adds external memory beyond the embedded flash needs to use a chip-select line to select that external memory. For this purpose, GPIOs 13, 14 and 15 are available to be designated as chip select lines. If your design implements one or more memory expansions, you will need to dedicate the appropriate GPIOs. For this purpose, be sure to consider future needs. The internal flash of the GSP3f chip is 4 Mbits, and internal RAM is 128 Kbytes. Of this memory, SiRF's software uses a significant portion (the specific amount varies with the software selected, and with options implemented – contact your SiRF technical support engineer for details of your system). If you plan to add significant software, or use flash memory to store data, be sure to allow for the possibility of memory expansion.

5. DOCUMENT MAINTENANCE

5.1. Required Approval for Changes

Changes to this document require the approval of Field Application Engineering, Marketing and Quality.

5.2. Revision History

Rev	Rev Date	CN Number	Description	Author/Editor
0.1	7/26/04	N/A	Preliminary Release	Carl Carter
1.0	4/4/05	2698	Initial Release under CN Control	Carl Carter

6. Appendix A – Consolidated GPIO Characteristics

GPIO	Alternate Functions[1]	Pad Characteristic[2]	Default Direction[3]	Register Access[4]
0	(None)	100 kΩ Pull Down	Input	Dir/Val 0 0x0080
1	Odometer Input	100 kΩ Pull Down	Input	Dir/Val 0 0x0040
2	AGC PWM	100 kΩ Pull Down	Input	Dir/Val 0 0x0020
3	SPI SSn[0]	100 kΩ Pull Up	Input	State 1
4	SPI SSn[1], MAG	None	Input	State 2
5	SPI SK	100 kΩ Pull Down	Input	Dir/Val 0 0x0004
6	SPI S0	100 kΩ Pull Down	Input	Dir/Val 0 0x0002
7	SPI SI	100 kΩ Pull Down	Input	Dir/Val 0 0x0001
8	RFPWRUP	None	Output, 1	State 3
9	Timemark	100 kΩ Pull Down	Input	State 4
10	EIT[0]	None	Input	State 5
11*	(Reserved)			
12*	(Reserved)			
13	CS[1], nCTS	None	Input	State 0
14	CS[2], nRTS	100 kΩ Pull Up	Input	State 7
15	CS[3], YCLK	100 kΩ Pull Up	Input	State 8

Notes
* GPIO pins indicated with an asterisk are reserved for use in future chip designs.
[1] First-listed alternate functions are selected using the GPIO Select register. If a second alternate function is listed, it is selected using bit 13 of the associated GPIO State register.
[2] Pad characteristics indicate internal connections to the GPIO pin.
[3] Default direction at reset.
[4] State *x* means that GPIO State register *x* controls this GPIO. Bit 14 sets the direction (0=input for most, 1=output; GPIO 8 0=Tri-stated, there being no input capabilities), Bit 15 reads the value when input, sets the value when output. For pins with secondary alternate function, bit 13=1 selects the secondary alternate function. When using secondary alternate function, direction must be correct. For GPIOs 4, 13 and 15, direction must be set to input; for GPIO 14, direction must be set to output for secondary alternate function to work. Dir/Val *x 0x00xx* specifies the pin is controlled by two registers: GPIO_PortDir*x* and GPIO_PortVal*x*. Within each register, the bit designated by *0x00xx* controls that GPIO. In the GPIO_PortDir register, setting the corresponding bit to 1 indicates the port is an output, 0 sets it to an input. Within the GPIO_PortVal register, the corresponding bit mirrors the state of the input when the pin is in input mode, and sets the state when the pin is set to output mode. By default, all Dir/Val registers have a reset value of 0, indicating all are set to input direction.