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# SiRF Application Notes
# Troubleshooting Note for SiRFstar III Board Development

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**LIST OF FIGURES:**

# 1. PURPOSE

The purpose of this document is to provide insight and instructions on how to troubleshoot problems associated with GPS modules using the SiRF SSIII chipsets.

The document contains information on a list of troubleshooting steps while debugging. There are two sections for Troubleshooting within this procedure. Section 4 covers Basic Troubleshooting and should be used first by Production Technicians in order to fix and repair failure boards faster. Section 5 and 6 gives a detail explanation that can be used by Test Engineering to support production Technicians.

# 2. Scope

It is important to have an understanding of the most common causes of basic problems associated with GPS modules. Almost all operational problems of a GPS module can be traced to the following categories:

- Incorrect or improper choice of components (BOM)
- Incorrect or improper placement of components
- Incorrect or improper engineering practices
- Defects in manufacturing
- Incorrect, insufficient, or noisy supply voltage
- Incorrect or incompatible operating firmware installed
- No firmware installed
- Incorrect configuration settings
- Insufficient or poor quality clock sources
- Insufficient RF input to the module
- In-band noise or an RF jamming signal present
- Human error in connections or operation

# 3. REFERENCES

## 3.1. Documents

### 3.1.1. Industry Standards

QASD0001, Quality Policy Manual

### 3.1.2. Applicable SiRF Reference Documents

SSIII Reference Designs

- GSP3e + GRF3W (2010-0119) Schematic
- GSP3f + GRF3W (2010-0125) Schematic
- LGA Carrier Board SSIII (1060-0122) Schematic
- S3SLC100 Evaluation Receiver (1060-0120) Schematic
- GSP3f Datasheet
- GRF3w Datasheet
- APTN3001 SSIII System Design Guidelines and Considerations
- APNT3002 PCB Design Guidelines for SSIII Implementations
- APNT3004 Co-Location and Jamming Considerations for SSIII Integration
- APNT3005 GPIO Functionality for SSIII
- APNT3008 Power Management Considerations
- APNT3009 Production Testing of SSIII Modules
- APNT3010 SPI Interface Issues for SSIII
- APNT3012 System Validation Techniques for SSIII
- APNT0022 Integrating Patch Antennas with SiRF GPS Receivers

# 4. Requirement

## 4.1. Equipment Needed

- Oscilloscope, > 100 MHz BW

- Digital Multi-meter
- GPS Satellite Simulator or live GPS satellites with active antenna feed
- Satellite re-radiator where applicable
- Frequency Generator (HP8662, HP8663, or equivalent)
- SSIII LGA Carrier Board (2010-0122) or equivalent interface board
- Spectrum Analyzer
- RF Network Analyzer

# 5. Basic Troubleshooting:

If your "device under test" (DUT) or board fails the functional test, then you can use the following guidelines to rule out any simple problem.

## 5.1. Troubleshooting Procedure: (Initial Check)

- Check for proper voltage and current levels at the input to the board. If the DC current exceeds 150mA at 2.85v during initial satellite search, there is probably a problem, possibly a short somewhere. In this case, visually check for short circuits or improperly placed components.
- Verify that the input voltage to the RF device is approximately 2.85 VDC +/- 5%. **Note: Exceeding 3.15VDC will damage the GRF3w device.**
- Verify that the GSP3 Baseband chip input voltage (VDD) is 2.7VDC to 3.6VDC, and the GSP3 Baseband chip RTC voltage (VDDRTC) is 1.4VDC to 1.6VDC.
- Verify that the GRF3w XTALIN reference level is between 200mV to 1200mVpp. Note: A FET Probe is recommended for this measurement.
- Verify that the GRF3w XTALIN is between 13MHz and 26MHz. and the proper "pull-up" and "pull-down" straps are in place per the recommended reference schematic.
- Test whether the RF section is generating the proper reference oscillator frequency (std ref_freq = 16.369 MHz) by measuring ACQCLK.

-- The acquisition clock as measured at the interface between the RF chip and baseband chip should be 16.369 MHz.(CMOS level). This interface line is referred to as ACQCLK.

- If the frequency is not as listed above or if there is no clock signal, then check the oscillator components and associated circuitry such as Loop Filter for PLL. The system cannot run without the proper clock.

**Note: A 0.5ppm TCXO is required for SSIII designs.**

- If the DUT is not communicating with the PC, then:
  - Ensure that the firmware has been programmed onto the flash of the GSP3f, and the system is properly configured based on the desired reference clock used.
  - Check that you have the correct configuration setup: See "Notes on Configuration Options" below.
  - Check that the system is in data mode, and not in boot mode:
  - Ensure that you are utilizing a CMOS to RS-232 level shifter to convert from the SiRF CMOS output on the UART of the baseband, into RS-232 to speak with the PC.
  - Ensure that comm. port selected in SiRFdemo is properly connected to the UART-A of the GPS board.
  - Ensure that you have synchronized the baud rates between the PC and the DUT. SiRFDemo can be used as a tool under the "Actions" menu to synchronize. See 6.1.1.2
  - Check TXA and RXA, for activity. You should see short bursts of data every second from the TXA line. Use an oscilloscope to check for these short bursts by probing the TXA and RXA test points at the I/O connector.
  - Ensure that the power supervisor or reset circuitry is in place and properly applied.
- If the unit is failing due to poor RF sensitivity. Visually check for solder bridges, loose or bad cable connections, wrong parts and other similar problems.
- If an RF Network Analyzer is available check that the gain from the antenna-input to the input matching network of the GRF3w is approximately 13 to 26dB depending on the type of LNA and SAW filters used.
- Poor RF sensitivity can also be caused by poor TCXO phase noise. Verify that the phase noise of the TCXO is within the specified limits.

## 5.2. NOTES ON CONFIGURATION OPTIONS

The SSIII product line has several configuration options. The three main configuration options are "power management", "GPIO functionality", and "Boot Clock". For reference to these options please refer to APNT3005 GPIO Functionality for SSIII, APNT3008 Power Management Considerations and/or APTN3001 SSIII System Design Guidelines and Considerations.

If your board is not configured correctly, damage could result, or the board may simply not work. Refer to the bill of materials and schematics for the option that you are building. The bill of materials only shows parts that are to be installed**. There may be a different bill of materials for each configuration option**.

The schematic shows all the parts that the PCB was designed for and should be used only for troubleshooting, not assembly. The assembly drawing also shows all the parts and should be used to see where the components are placed, but not which components to install. Latest available configurations to date are posted on the SiRF Customer Development Site.

Configuration Example: With the Address and Data pins.

| Signals | Descriptions |
|---|---|
| ED0 | Read on power up to determine boot (1=internal, 0=external) |
| ED1 | (1=GRF3i selection) |
| ED2/ED3 | Read on power up to determine Boot Clock Selection: |

| ED3 | ED2 | |
|---|---|---|
| 0 | 1 | = RTC Clock |
| 1 | 0 | = ECLK |
| 1 | 1 | = ACQCLK |

Configuration Example: With the Debug interface pins. During "boot-strap these pins determine GRF3w reference frequency.

| Signals | Descriptions |
|---|---|
| JTCK & JTDI | During "boot-strap these pins determine GRF3w reference frequency. |

| JTCK | JTDI | |
|---|---|---|
| 0 | 0 | = 16.369MHz |
| 0 | 1 | = 24.5535MHz |
| 1 | 0 | = 26.0MHz |

**Note: Be sure configuration options are connected to the latest revision. Contact SiRF customer support if assistance is required.**

# 6. Digital Section

The following notes assume that the receiver has failed some initial testing using SiRFtest and a single channel signal generator or live satellites. For RF troubleshooting/GPS performance issues, see the RF section.

## 6.1. Typical Symptoms

Unit fails to output data (no display on SiRFDemo).

### 6.1.1. No Communications with PC

Check TXA and RXA, for activity. If you see short bursts of data every second from the TXA line, after the reset is activated, then unit is running and outputting data. The SiRFdemo program may not detect the data because the baud rate is wrong or the wrong COM port on PC has been selected. See 6.1.1.2

#### 6.1.1.1.NMEA Default

If the board is programmed with NMEA output as the serial protocol, the serial port settings on the SiRFdemo must be changed to 4800 baud, No Parity, 8 Data bits, 1 Stop bit. Enable the "Development Data" window on the SiRFdemo program to see the raw data output by the receiver. After the NMEA messages are displayed (all start with $) then switch the mode to SiRF Binary format using SiRFdemo for detailed view of signal levels, satellites tracked, etc. Another serial communication program could also be used (HyperTerminal, ProComm, etc.) to monitor the output data.

**Note: The default baud rate for SSIII NMEA is 4800 baud.**

#### 6.1.1.2. SiRF Default

The SiRFdemo program will not display data if the baud rate is wrong. The default serial port settings for SiRF binary mode is 57600, N, 8, 1. The easiest way to synchronize the baud rates between your DUT (Device Under Test) and SiRFDemo is to use the "Actions" menu in SiRFDemo, and choose the "Synchronize Protocol and Baud Rate" option. SiRFDemo will synchronize with the DUT and then switch it to a common 57600 baud rate. As a note, if you are experiencing erratic, incorrect baud rates, or baud rates other than what has been defaulted in your modified code, then you must consider clearing the on chip SRAM of the SSIII baseband chip. Battery backed SRAM will store the last settings used, prior to power down if the proper battery back up voltage is present.

#### 6.1.2. No Activity on the TX Line.

Most likely problems:

- The SiRFstar program in the FLASH is corrupt, but the boot code is ok.
- The Flash is not programmed, or programmed incorrectly.
- The processor does not have a proper clock.
- Incorrect configuration setup.
- Incorrect Boot sequence
- The APM_INTR "ON_OFF" line is logic high. Note: The "ON_OFF" must be low during power up and remain low at all times except during APM wake-up. If this signal is allowed to go high it can not only affect activity on the TX line but also inhibit the baseband regulator from turning on.
- The PWRCTL "nWAKEUP" line is logic high.
- Bad solder joint. Note: Modules may need to be x-rayed if BGA devices are used.

##### 6.1.2.1. The Flash is not programmed, or programmed incorrectly.

No activity on the TX line could happen if FLASH is blank or corrupted code was installed. Using SiRFflash, put the DUT into boot mode (data line 0 is pulled high) and attempt to Flash with a proper SiRF .s file. Note: SiRFflash does not require loaded flash to work. SiRFflash interfaces with the boot code on the internal ROM of the baseband chip to begin the flashing process.

**Note: A proper version of SiRFlash is required. Refer to the customer development site for Firmware compatibility information.**

##### 6.1.2.2.The Processor does not have a proper clock

Power management must be configured and connected correctly and proper clocks must be present for proper system boot up and operation. If there are any problems in the power-up sequence, the configuration, clock generation and battery back-up power considerations should be thoroughly reviewed.

The clocks are the heart of a GPS system. Ensure that the RTC oscillator and ACQCLK are toggling at their specified rate and with sufficient amplitude. If ACQCLK is not present then check for proper programming and boot up of the GRF3w chip and proper SPI connections between the RF and baseband.

Note: There are three different possible boot-up configurations, Boot from RTC, Boot from ECLK, and Boot from ACKCLK. Refer to APTN3001 SSIII System Design Guidelines and Considerations for information on the design steps to insure proper operation on the type of boot sequence selected.

#### 6.1.2.3. Power Management:

Please refer to application note APNT3008 Power Management Considerations for additional information on power management operation.

**Note: In general, power management is primarily controlled by the RTC finite state machine (FSM) and the RTC SW control registers. The control is managed by a combination of GPIO toggling to control registers (via the FSM of nWAKEUP and ON/OFF), and some SPI interfacing. It is important to have correct "toggling" configuration. Below is a sample of such configuration:**

**GSP3f Power Management States/Configuration**

| State | nWakeUP | GPIO8 | GPIO0 | ON/OFF |
|---|---|---|---|---|
| Full Power | L | H | H | L |
| CLK Only | L | H | L | L |
| Stand By | L | L | L | L |
| Hibernate | H | L | L | L |

#### 6.1.2.4.Incorrect RTC Start Up Sequence

Verify that the "power on reset" circuit, POR transitions Low, nSRESET transitions High and the RTC clock is present and stable after power up or system reset.

#### 6.1.2.5.One or more control or clock lines are shorted together

This can cause the processor to hang up during or after starting. If the clock is good, and the configuration resistors are ok, then verify no shorts on address/data/control lines.

#### 6.1.2.6.Bad Solder Joint

If there was not enough solder paste applied, some bad solder joints may be causing the problem. Inspect under a microscope and touch up any suspect areas. As mentioned above, modules may need to be x-rayed if BGA devices are used.

# 7. RF SECTION

## 7.1. Typical Failure modes

There are 4 basic RF related failures that typically occur. These are:

1. No signal acquired
2. Low C/No
3. Incorrect selectable clock configuration
4. Unstable navigation

- If there is no signal acquired there is usually a gross functional failure. The steps below should point out the problem, or show which section has failed.

- For Low C/No there are usually three causes: front end gain/Noise Figure issue, a VSWR mismatch issue, or self jamming. Even if these sections have component or connection failures, enough signal can pass through to allow the system to work, but with a degraded C/No.

- Incorrect clock configuration, a poor clock, or mistuned clock frequency will cause long TTFF's and perhaps an inability to acquire any satellites.

- RF related failures can also be caused by the PLL in the GRF3w not being locked. Verify proper component values in the loop circuit and a loop voltage of between 0.5v and 2.2v. Incorrect or misconnected loop filter components can contribute to longer TTFFs and degraded C/No.

- Finally, unstable navigation will occur if the crystal is not providing a clean frequency source, or if the Vcc supplied to the RF section is not clean (free of noise), consistent and controlled.

#### 7.1.1. No signal acquired

There are several reasons why your board may not be receiving a signal. However the most fundamental reason is insufficient GPS RF signal in. Ensure the proper RF input is supplied to the DUT and that the LO signal is the proper frequency and level. Do not rely on an antenna placed near a window for proper GPS satellite visibility. Compare with a SiRF Evaluation Kit if in question.

##### 7.1.1.1. Incorrect RF input to the module.

If you are connecting the signal source via a GPS simulator onto a board, ensure that you have a proper mate from the simulator to the board connector. Do not mix and match connectors. As well, the board connector must have a proper ground and center conductor connection.

If you are testing with an antenna, there are a couple of things to keep in mind.

(a) The center frequency of the antenna. Ensure that you are using a proper 1575.42MHz centered antenna. For further information pertaining to antenna tuning, see SiRF application note APNT0022.

(b) Is the antenna an active antenna? If you do not have an LNA on the GPS board and you are using an active antenna (LNA in the patch antenna assembly), then you must ensure that the proper voltage source is provided to the active antenna.

(c) Use of a DC block between the receiver and the antenna is recommended if the antenna supply is not needed from the receiver.

##### 7.1.1.2. Incomplete RF path

If you are still not seeing a signal into the SiRF RF chipset, then the following exercise may help pinpoint the source of your problems. Assemble a small PC board with an LNA, characteristic of the LNA used in SiRFstar reference designs. On the input of the board is a connection to supply a GPS carrier signal, and on the output is a coax, with the conductor exposed.

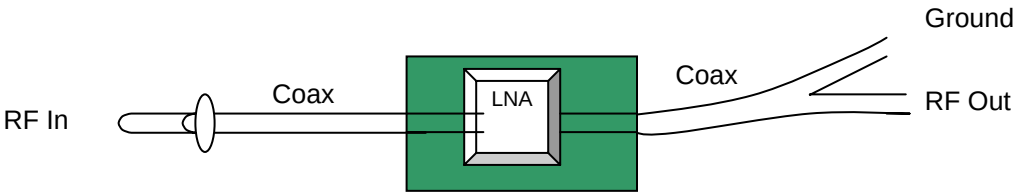


**Figure 1 LNA Test Board**

With this setup, begin at the RFin pin of the SiRF RF chip. If you can establish a signal and a navigation solution with the direct connection into the RFIN pin, then move the LNA test board back through the RF system. Establish a fix at each subsequent RF stage, until you encounter an inability to achieve a fix. This will expose the area which is causing the issue.

The final test, is to look for certain interface clocks to be present, between the RF chip and the baseband chip. The CLKACQ is derived from the VCO by dividing 49.107MHz by 3. The frequency on the CLKACQ should be 16.369 MHz. If it is not, then the PLL is not working correctly. If all other clock considerations are correct and intact, then the only place for a problem is probably the loop filter, which will limit the issue to checking the off chip components which constitute the loop filter, or replacing the RF IC.

### 7.1.2. Low C/No

Using a signal generator (or a GPS signal generator with the code and data modulation turned off) inject a signal in the RF input at –100 dBm. Using a 10x-scope probe monitor the signal on the SIGN pin of the RF chip with a spectrum analyzer. Set the center frequency of the spectrum analyzer to 3.996 MHz. (The IF of the SSIII is 3.996MHz). Set the span to 1 MHz. Typically there should be a carrier shown with a carrier to noise ratio of 25 to 30 dB at 80 KHz away from the carrier. (RBW=10 kHz, IF averaging on) Zoom in on the carrier to at least a 1 kHz span, and ensure there are no sidebands, or jumps occurring. If there are sidebands, it is an indication of noise coupling into the front end, or noise coupling into your antenna. Also place a well-characterized LNA (Gain of 20dB or more and Noise Figure of less than 1.5dB) and a filter in front of the receiver. If the signal to noise increases significantly the RF front-end amplifier is not functioning properly. If this test does not improve the signal to noise ratio, then look for spurs within +/-10MHz of the carrier. Keep in mind, the off chip LNA is primarily used to set the Noise Figure (NF) of the system.

If possible measure the Input Return Loss of the LNA with a network analyzer. It should be better than 8 dB. Make sure the power from the analyzer is not overdriving the front end LNA. (<25dB of gain) This will distort the reading.

VSWR={1+√(Reflected Power/Forward Power)}/{1-√(Reflected Power/Forward Power)}

### 7.1.3. Mistuned Reference Clock

SSIII architecture utilizes a TCXO or temperature controlled crystal oscillator only design.
a) The standard design uses a 13MHz to 26MHz external reference oscillator with a typical +/- 0.5 PPM swing.
b) The SSIII frequency configuration selection must be correct per the boot up mode selected. (See Chart below for configuration strap selections)

| Frequency | Signal |
|---|---|
| 16.369MHz | JTCK = 0 & JTDI = 0 |

**24.5535MHz JTCK = 0 & JTDI = 1**

**26.000MHz JTCK = 1 & JTDI = 0**

**Note: If any other reference clock frequency is to be used, please refer to the customer developer's site or APTN3001 for configuration settings.**

### 7.1.4. Unstable navigation

VCO Unlock messages occur when cycle slips occur. A slipped cycle occurs due to a problem in the oscillator or clock sections. This causes the internal counters to glitch.

As well, Parity Error messages can occur when a satellite is marginal. This is normal for satellites that are fading in and out near the horizon, or are being blocked. If the message occurs for all satellites at once then this indicates a crystal problem. Bit Edit errors also occur if the crystal reference is too noisy. The most likely reason for this is a poor quality external frequency source. GPS systems need very low noise clocks, and many manufacturers can not make oscillators suitable for GPS. Where possible, use the same TCXO as listed on the SiRF bill of materials, supplied with the reference designs.

To ensure that your chosen GPS reference source and layout are stable, test your board design against a SiRF EVK, or versus one of your board's with the TCXO replaced by a directly injected clock source. Use a frequency generator and input a 300 to 600mVpp sine wave directly into the XTALIN pin. Be sure the injected source is the same frequency in which the system is configured for.

### 7.1.5. TTFF "Time to First Fix"

To properly troubleshoot a TTFF problem, it is important to understand TTFF and the different start up modes. The three main TTFF modes are Cold Start, Warm Start, and Hot Start.

- Cold Start – To start the GPS receiver with no previous position, time or ephemeris information. If the receiver fails this mode, check all of the above sections for compliance.
- Warm Start – To start the GPS receiver with position and time, but no ephemeris. If the receiver passes cold start but fails warm start, check that proper position and time information are present.
- Hot Start – To start the GPS receiver with position, time, and an ephemeris that is less than four hours old. If the receiver passes cold start and warm start but fails hot start, then verify proper battery back up voltage is present.

### 7.1.6. Temperature Concerns

If temperature extremes appear to be a problem where the module operates to specification under ambient conditions but fails under hot or cold temperature variations, perform the following checks.

- Verify the temperature extremes are within the operating specifications as indicated in the SiRF Data Sheets.
- Stress the module in the temperature direction (hot or cold) in which the failure appears. This can be done either by using a temperature chamber "electronic freeze spray" or wrapping the module in plastic and running it for a period of time without ventilation allowing it to get hot.
- While the module is being stressed, monitor the reference clock and the critical voltages for variations. These are the most sensitive areas under temperature extremes.

### 7.1.7 Jamming Concerns

If sensitivity is poor and all above RF related concerns have been addressed there may be a possibility of EMI or jamming. See APNT3004 Co-Location and Jamming Considerations for SSIII Integration as a reference.

If a problem exists that is related to jamming, the jamming source may be external coming in through the antenna input or it may be internally generated through noise or other co-located circuitry. In either case there is a test software version that a customer may load into the SSIII receiver enabling an IF measurement. This measurement is internal to the RF device and can help isolate a possible jamming condition.

The software (Version HS3_C13_Flash.s) can be obtained through SiRF Applications Engineering and loaded into the GPS receiver using SiRFFlash.

**Note: A proper version of SiRFlash is required. Refer to the customer development site for Firmware compatibility information.**

The main purpose of this software is to activate TP_IF pin #31 on the GRF3w RF device. Under normal operating conditions with standard SSIII software the TP_IF pin is not activated in order to reduce current consumption. Once activated post-mixer IF measurements can be made using a wideband FET probe (BW>500MHz) into a spectrum analyzer. Figure 2 is an illustration of such measurements under terminated, no jamming, and simulated in-band jamming conditions.

For spectrum analyzer set up follow the settings as listed in Figure 2 for, ref level, center freq., span, etc., measure the output of both the sign and TPIF pins and compare with the plots as listed below. The top waveforms are for the sign measurement and the lower waveforms are for the TPIF measurement. The lines displayed in Figure 3 represent the various conditions for evaluating jamming concerns. With the antenna input of the receiver terminated, the waveforms should be as illustrated. If internal jamming is present spikes or peaks should be evident. With an antenna connected and no jamming present, the waveform should be similar to the "dashed" line with no peaks or spikes. If peaks or spikes are present then most likely jamming is entering through this path.

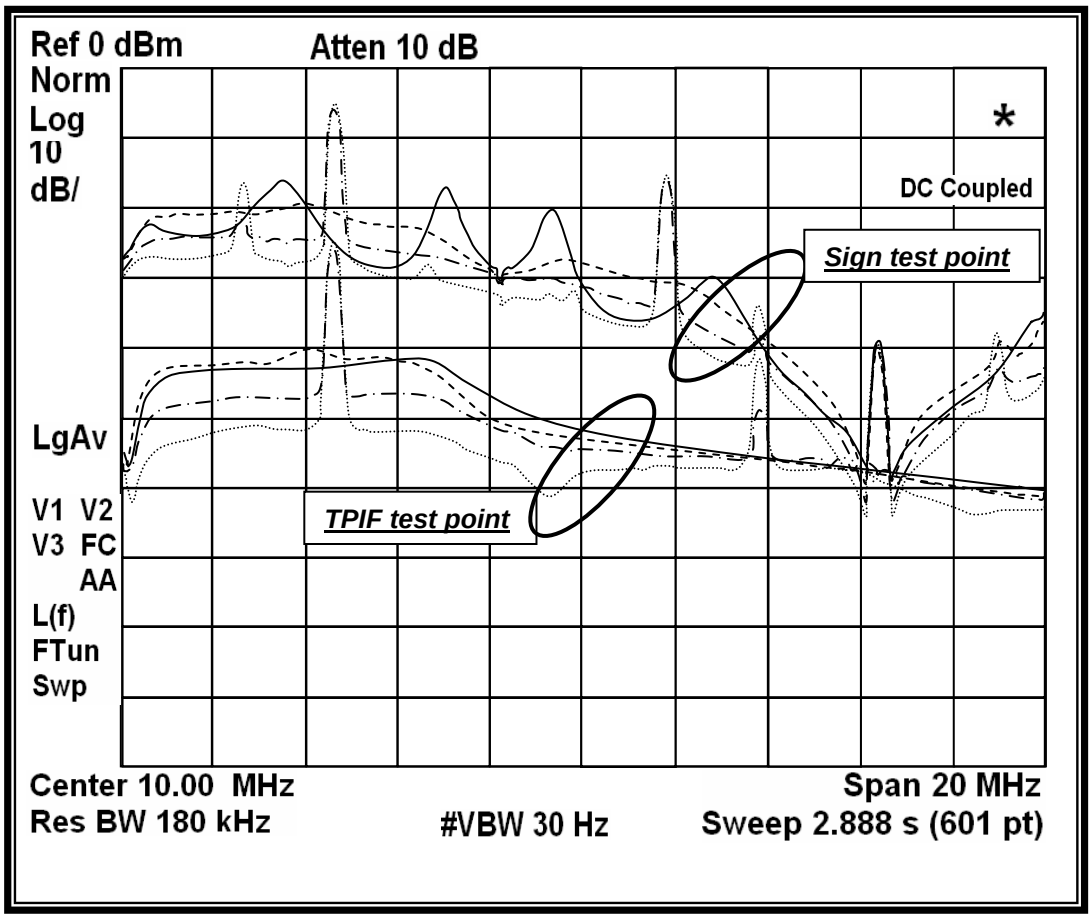


**Fig 2**

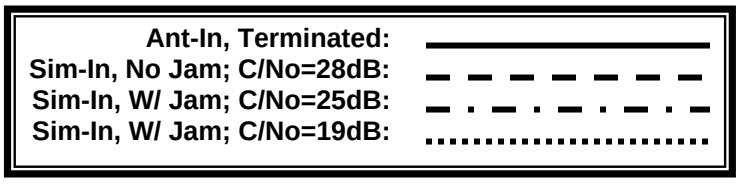


**Fig 3**

# 8. DOCUMENT MAINTENANCE

## 8.1. Required Approval for Changes

Changes to this document require the approval of Marketing and Operations.

## 8.2. Revision History

| Rev | Rev Date | CN Number | Description |
|---|---|---|---|
| 0.0 | 9/10/2004 | N/A | Preliminary Draft |
| 1.0 | 2/2/05 | 2655 | Release under CN Control |