# SiRFstar III System Guidelines and Considerations

(For GRF3w Design Related Implementations)

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# 1. Introduction

This document discusses the suggested system design guidelines and considerations for implementation of the SiRFstar III chipset, hereafter identified as the GSP3f Baseband processor with integrated Flash memory, and the corresponding GRF3w RF front end. This set is considered the first generation of chip options available for the SiRFstar III family of chips. Future generation of chipsets will be discussed in subsequent APNT releases.

## 1.1. Background

The initial focus of this document will center on the GSP3f chip, the pin functionality and the key design considerations. Where possible, attempts to clarify the functionality in autonomous mode and aided mode will be noted. Subsequent sections will discuss the interface to the GRF3w RF chip. In addition, the design implementations and considerations that must be addressed during system configuration and advance planning, front end options and integration/ packaging issues. Radio co-existence considerations will also be partially discussed.

# 2. References

## 2.1. Glossary of Special Terms

**APM:** Advanced Power Management. The mode of low power management used in conjunction with SiRFLoc 3.x software. Update rates are limited from 10 seconds to 255 seconds. The software evaluates the signal environment, and adjusts for full power when needed. Used with SLC3 aided code.

**ATP:** Adaptive Trickle Power mode. The mode of low power operation that intelligently switches between trickle power and full power depending of signal strength to minimized low power operation. Typically defaults to full power operation at signal levels of <28dB Hz. Used with standard GSW3 code.

**BIU:** Bus Interface Unit: Internal controller subsection of the GSP3f.

**FSM:** Finite State Machine: Advances the low power RTC based circuit in certain modes and states.

**GSW3.x:** Autonomous operation software: Term defining standard, autonomous software used for SiRFstarIII receiver operation, version 3.x.

**HIBERNATE STATE:** A very low power standby state under future development by SiRF. Sometimes referred to as "Extreme Low Power". Allows for faster startup during periods of deep sleep.

**SLC3.x:** Aided operation Software: Term defining the operation of aided SiRFLoc Client 3.x software operation with the SiRFstarIII receiver. Also referred to as "Multimode".

**POR:** Power on Reset: An externally generated active low signal used for system reset.

**PTF:** Push-to-FixTM: A power savings mode characterized by infrequent power-on times, and allows for a push button fix in 2 to 8 seconds, on demand.

**RTC:** Real Time Clock: Circuit used to keep current time when the main power to the receiver is off.

**RTCM:** Radio Technical Commission for Maritime Services. A protocol for transfer of differential GPS corrections.

**STANDBY STATE:** (Also called Trickle Power) The mode of power management where the RF power is off (for the 3w) and the Baseband power is ON, but no clock is executing processor activity. This requires about 700uA of current, typically.

## 2.2. Industry Standards

Additional documents will be referenced at a future time.

## 2.3. SiRF Documents

**APNT 3002**: PCB Design Guidelines for SiRFstar III Implementation

**APNT 3003**: Troubleshooting Notes for SiRFStar III Implementation

**APNT 3004:** Co-Location and Jamming Considerations for SiRFstar III Implementation

**APNT 3005:** GPIO Pin Functionality for SiRFstar III Implementation

**APNT 3008:** Advanced Power Management (APM) Considerations for SiRFstar III

**APNT 3009:** Production Testing of SSIII Modules

**APNT 3012:** System Validation Techniques for SSIII.

**APNT 3014:** SiRFLoc Aiding Considerations

**GPS Clock Specification for the SSIII System**

**SiRF Reference Design Schematics 1060-0122 and 1060-0122**

**SiRF SDK Users Guide**

**SiRFlash 2.14+.**

**SiRFDemo 3.75+:**

## 2.4. Appendices

Appendix A: Recommended Solder Pad Footprints
Appendix B1: Recommended External SRAM Connections
Appendix B2: B3, Buffers Circuits
Appendix B4: Boot Up Sequences, In Detail.
Appendix C: Special Pin Functions and Cross Reference Table

Appendices A, B and C are noted at the end of this document.

# 3. The GSP3f Baseband Processor and Interfaces:

The GSP3f processor chip integrates an ARM7TDMI CPU, along with 4Mb of internally packaged Flash memory. This is a 20 channel capable receiver with matched filters to offer over 200,000 effective correlators for advanced signal processing which offers excellent improvements in the time to first fix (TTFF), and much lower signal sensitivities.
The high degree of versatility in this chip allows for a wide array of GPS product implementations, and the ability to use the ARM processor for additional non-GPS applications.
The baseband processor structure is somewhat similar to earlier SiRFstarII designs from the standpoint of RTC operation, battery backup requirements, ARM functionality and some GPIO functionality. The details of the actual changes will be outlined in later sections in this document. A primary difference to note here is that the internal DSP core, the RTC state machine and the 4 kbytes of battery backed SRAM (BBRAM) now run at 1.5VDC, instead of the 1.8VDC supply previously required in the 2e/LP chip.
Another key change that has occurred is the elimination of the PECL interfaces for CLK, SIGN and MAG data lines. Therefore, the need for PECLREF is not required. Since the new interfaces are CMOS logic levels typically operating at 2.85V, special care must be taken during the layout to properly isolate and shield these lines. The dV/dt edge rate swings are higher, and the possibility of higher EMI levels should be taken into consideration during layout, and additional system EMI measurements should be verified in each end users platform.

Implementation into the smaller 8x8mm package limits the number of available pins, and has thus limited the direct pin assignment and GPIO availability. Therefore, many functions have become 'shared' functions that are defined during the initial boot sequence. Most of the shared pins default to the GPIO state during bootup. Please refer to Appendix C at the end of this document for pin names and cross functionality. Additional details of the shared GPIO functions can be found in APN3005, GPIO Pin Functionality for SiRFstar III.

## 3.1. GRF3w RF Front End Interface

It is important to note, that with the GSP3f Baseband engine, many different RF reference clock frequencies can be selected due to the unique fractional-N capabilities available with the GRF3w RF chip. Please note that the GRF3w must be initially programmed into the correct divider configuration by a 3-wire SPI port. This mandates that a stable clock be present to the GSP3f chip from some other source during boot-up to allow for proper GRF3w programming. Initial software releases will allow for a boot from RTC approach, and the choice of various reference clock frequencies can potentially be selected by using the proper resistive pull-ups/downs. Boot from ECLK and other sources are possible, and may be addressed in subsequent software releases. Use of shared clocks for ECLK power management and timing requires advanced planning and development.

### 3.1.1. Reference Clock Changes

The GSP3f chip no longer relies on the doubled 49MHz GPSCLK supplied from the RF chip. There is now an internal PLL function to allow for frequency multiplication of the acquisition clock (CLKACQ) supplied from the GRF3w. This provides for more versatility in core processing speed, since the doubler that was available in the previous 2i/LP design, is no longer implemented.

This provides the developer more versatility in choices of processing speed vs. power consumption tradeoffs, and will become more evident in later system configurations.

### 3.1.2. AGCDAT

AGCDAT is driven by AGCPWM and is an input. It is a narrow pulse used to control the gain of the IF AGC loop. It is controlled by a 5 bit word, and is a CMOS level signal relative to VDD.

### 3.1.3. SPI Interface

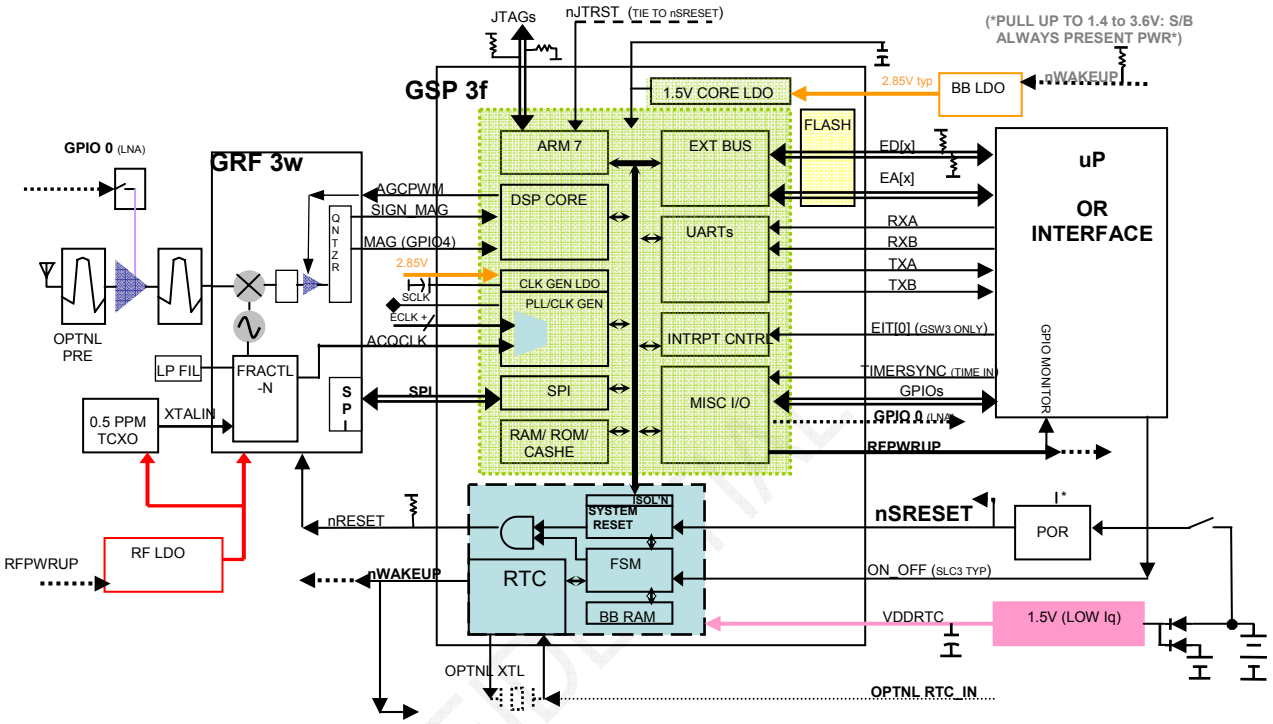
The SPI interface is also at CMOS signal level, and is used to program the chip for proper fractional N frequency control, and power management.

### 3.1.4. nRESET, SIGN, MAG & CLKACQ

The nRESET pin (also referred to as RSTB) is a level sensitive input that is used to put the chip into a standard default state when coming out of a sleep mode. A minimum of 1ms low is required to properly set the default state. The threshold voltages of nRESET are VCC*0.2 min and VCC*0.8 max. It is driven by the open drain output of nRESET, and requires a minimum of a 10k pull-up to VCC.
The SIGN and MAG outputs are receiver data samples, and are CMOS outputs used to drive the GSP3f chip.
The CLKACQ output is a 16.369MHz CMOS clock output that is the reference for the baseband signal processor. It is derived from the divided LO of the GRF3w fractional N synthesizer. Keep this trace short, clean and well isolated.

## 3.2. Block Diagram of GSP3f with GRF3w

A block diagram of the GSP3f chip integrated with the GRF3w chip is shown below.




**FUNCTIONAL BLOCK DIAGRAM: 3w + 3f CHIPSET**

## 3.3. GSP3f Power Requirements

Since the GSP3f chip is designed using a lower voltage 0.13um CMOS process, new power supply considerations are in order. For lowest power, the recommended voltage requirements are as follows (-40C to 85C):

| | | | |
|---|---|---|---|
| Core Power | VDDK | = 1.50V nominal [1] | (1.40V < VDDK <1.60V) |
| RTC Power | VDDRTC | = 1.50V nominal [2] | (1.40V < VRTC <1.60V) |
| I/O Power | VDD | = 2.85V nominal [3] | (2.70V < VDD <3.60V) |
| Flash Power | VDD | = 2.85V nominal [3, 4, 5] | (2.70V < VDD <3.60V) |
| Other Power | VDDx | = 2.85V nominal [3, 4, 5] | (2.70V < VDD <3.60V) |

**POWER NOTES**: Referenced at 25C, unless otherwise noted.

1. Total receiver power can be expected to run in the ~75mA range (from a 2.85V supply) during the initial acquisition search mode. A peak current surge of 12mA (or more) can also occur during initial acquisitions, and is also a function of the regulators used. This higher current requirement can last from tenths of seconds, to several seconds or more depending on signal strength and accuracy of aiding information. Average tracking current is ~65mA. More information is discussed in separate aiding applications, and power management application note APNT3008. The initial power supply ripple requirements are still TBD, but a reasonably safe value would be ripple for the 3f would be <5mVpp from DC to 3 MHz. EMI issues are still TBD. The RF power must be considerably cleaner, and is discussed later.
2. RTC power consists of: a.) RTC clock and state machine operational current, b.) BBRAM power and c.) STANDBY leakage effects. This can be expected to be <10uA during quiescent periods, and ___uA during brief BBRAM read/write operations. This power ring is totally independent of the core power. If one includes the ground pin currents required by the voltage regulators in sleep mode, then this value can be expected to add to the total needed by anywhere from 4uA, to 'x'uA higher. Special considerations relative to transients on this line during battery backup switchover should be minimized as much as possible. VDDRTC voltage ramp time should be <10ms and monotonic, free of any "multi-plateau" characteristics. The initial power supply ripple requirements are still TBD, but a safe value would be ripple of <1mV pp from DC to 3 MHz. A 2.2uF bypass is required on this pin. For additional low power concerns, refer to the special low power APM notes later is this document.
3. I/O power has been designed to operate from 2.7V and 3.6V. As of this writing, the GSP3f chip is still not fully evaluated for operation at 2.5V. For all operating conditions and best power /performance tradeoffs, we suggest operation at 2.85V. This I/O power ring is independent of all other power rings. The initial power supply ripple requirements are still TBD, but a reasonably safe value would be ripple of <5mV pp from DC to 3 MHz. Operation at voltages greater than 3.0V are potentially risky, due to the low voltage interface requirements of the new SiRF RF chips. The SiGe process limits the absolute maximum operating voltage of the RF front ends to 3.15V. Therefore, SiRF does not recommend any interface voltage greater than 3.0V for that reason. Use of baseband and RF power supply differences >0.25(TBD) Volts for non 3.3V tolerant inputs could cause latchup effects.
4. Flash power is usually in the ~15mA range during read/write. The flash is normally specified for operation down to 2.7V, and timing uncertainties at the lowest voltages is still under characterization. The initial power supply ripple requirements are still TBD, but a safe value would be ripple of <5mV from DC to 3 MHz. SiRF presently cannot guarantee operation for the GSP3f below -40C and at levels less than 2.7V. NOTE: Flash writes occur after a fix has been completed, therefore, the current needed during flash writes, does not affect the peak currents stated above.

5. The internal PLL regulator accepts inputs from 2.45 to 3.6V, and regulates it to 1.5VDC. Operation at the temperatures extremes may introduce some timing problems on a very small percentage of parts when using the minimum of 2.7V. Characterization is in progress. SiRF presently cannot guarantee operation for the GSP3f internal core regulators if the input drops below 2.45V.
6. Power supply sequencing: It is important that RTC power is applied first, since the system reset is passed thru this section of the chip first. All remaining GSP3f and GRF3w power should come up at the same time if possible. More details regarding this issue is discussed later in this document.

Higher voltage levels can be used, but will require higher levels of current consumption. This is usually not desirable due to the higher power needed for operation.

Implementation of an external switcher could be considered for core usage to save on battery power, but this has not been fully characterized by SiRF to consider all possible EMI concerns, and thus the client should perform their own validation.

In addition, certain low voltage core GPIO's were designed to be 3.3V tolerant, because they may need to interface to systems requiring higher voltage swings or reference levels.

This information is referenced in **APPENDIX C** of this document.

### 3.4. Pin Definitions and Functionality

The shared electrical characteristics and pin functionality is also documented in **Appendix C** at the end of this document. A minimum configuration table for boot from RTC clock, and other clock frequencies, is shown below.

| ED[3] | ED[2] | BOOT CLK |
|---|---|---|
| 0 | 1 | =RTCCLK (std) |
| 1 | 0 | =ECLK |

| ED[1] | RF Chip Used |
|---|---|
| 0 | GRF3w |
| 1 | ALTERNATE GSC3 |

| ED[0] | Boot Source |
|---|---|
| 0 | External Boot |
| 1 | Internal Boot (flash load) |

**TABLE 3.4.1**

# 4. Outline of System Operation with the GRF3w RF Front End

The GSP3f architecture allows for a considerable degree of flexibility in reference clock selection and boot up options. Since the GRF3w RF chip has a Fractional-N synthesizer that is able to accept a clock from 13 MHz to 26 MHz, it is mandatory that the chip be programmed into the proper operating configuration as a primary requirement. This requires an available and known clock source (typically an RTC clock as a default) always be present during the nSRESET high transition to allow for a SPI programming sequence to begin. As previously mentioned, an external clock that is always available could potentially start the process.

For most customers, boot from RTC clock is the typical start up sequence. This requires that the RTC clock circuit be fully operational and stable when coming out of nSRESET. A surface mount RTC crystal should be used with the GSP3f chip, or the RTC reference clock could be provided externally. The RTC drive characteristics are discussed later in this document. Please realize that bootup and subsequent SPI programming sequence from an RTC clock will require slightly longer times than a faster clock could offer. The primary consideration that all customers must characterize is; the time required for the ultra low power RTC circuitry to start up and become stable and useable. At cold or hot temperature extremes, this could take several seconds. SiRF suggests that all customers perform adequate characterization of this phenomenon because it is dependent on several factors: primarily the speed of the initial voltage ramp to the VDDRTC supply (regulator and circuit dependent), gain characteristics of the oscillator cell, input/output capacitance, and the choice of RTC crystal used. Use of an adjustable power on reset (POR) supervisor may be desirable until characterization can determine an average statistical time for clock stability in all conditions.
The choice of clock reference frequency and boot options is implemented with external pull-up/pull-down resistors on the JTCLK and JTDI lines. This is outlined in TABLE 4.0 below. An x denotes don't care (for reference, an internal 100k pull-up is present for lines 9-13).
Please note: This table defaults to RTC clock bootup (per pins ED[2], and ED[3]).

| Boot Clk Freq (MHz) | JTCK | JTDI | ED[13] | ED[12] | ED[11] | ED[10] | ED[9] | ED[7] | ED[3] | ED[2] | ED[1] | ED[0] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 24.5535 | 0 | 1 | x | x | x | x | x | 0 | 0 | 1 | 0 | 0 |
| 13.0000 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 16.3690 | 0 | 0 | x | x | x | x | x | 0 | 0 | 1 | 0 | 0 |
| 16.8000 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 19.2000 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 26.0000 | 1 | 0 | x | x | x | x | x | 0 | 0 | 1 | 0 | 0 |

**TABLE 4.0 Bootup Configuration Table**

If a customer desires, the alternative to consider is boot from ECLK. This option is supported in the first release of software, but is untested. Since most design implementations will integrate the GSP3f with other radios or subsystems, the possibility

of other CMOS available clocks must be evaluated for use. Other clock sources can be chosen for use via the internal "glitchless" mux inside the GSP3f, but these are limited to special applications. YCLK is available for those customers who choose to use alternate clock correction approaches, and are willing to pay slightly extra for a fast TTFF solution. This is addressed in a special white paper available at a later date from SiRF Engineering.
A brief discussion of the typical GSP3f + GRF3w RTC based **start up sequence** is as follows:

**(This assumes a 24.5535MHz, 0.5ppm reference TCXO is supplied).**
The POR generator output (nSRESET) goes low for ~280ms(TBD) initially [40 stable clock cycles minimum]. All power supplies and clocks should be stabilized.

1. nSRESET then transitions high, and all pull-ups/downs are latched into the internal registers of the GSP3f, and the boot clock source and frequency is determined at this point.
2. RTC clock is used to initiate the external Flash boot sequence.
3. RTC clock is used to program the SPI port of the GRF3w for the right frequency plan. This occurs in less than 150 (TBD)ms.
4. The GRF3w fractional N synthesizer has now been properly configured to generate CLKACQ at 16.369MHz, and a brief stabilization time is allowed in the code for synthesizer stability. This is all performed via the SiRF software.
5. Once stabilized, the internal 'glichless mux' in the GSP3f allows for a smooth transition from the RTC clock over to CLKACQ via SW instructions.

In future development, alternate clock paths for startup could be implemented. For example, if an external buffer is implemented to drive ECLK, then ECLK can be used to run the GSP3f chip directly, or the internal PLL that runs off of CLKACQ can be selected (via SW) to run the GSP3f chip at alternate frequencies when desired. A more detailed boot sequence is detailed in Appendix B4.

### 4.1. System Operation: Supplemental Comments:

The GSP3f internal MUX circuitry will first sense if the new clock is present, and is ready and able to allow for a successful transition.

If clock sensing is not successful, the transition handoff does not occur, and the initial clock is continued in use as the reference.

Some comments are in order here to help the user understand other factors of the system operation.

a) System reset (nSRESET) goes low for a minimum of >40bootclk cycles(=TBD)ms, assuming the RTC clock is selected for use via the external pull-up resistors. Initial, first time power-up at hot temperatures may take longer for the RTC clock to stabilize.

b) RF chip reset (nRESET) follows the characteristic of nSRESET, and is delayed approximately 30 ns. This reset is sometimes referred to as "RESETB or RSTB", and is used to reset the 3w chip. It MUST be pulled up to 3V maximum via a 10k resistor. The pull-up power must be present before nSRESET goes high.

c) nCS[0] drives nCS_F. Use of a zero ohm resistor between pins E6 and F8 for probing access is highly suggested for troubleshooting purposes.

d) JTRST is defined as active low, and must be connected to the nSRESET line for proper operation at boot up. The internal flash does not require reset function.

## 4.2. RTC Considerations and External Drive Requirements

The characteristics of the GSP3f internal RTC cell are as follows:

Standard Pierce oscillator cell at 1.5V. No active load bias used.

Gain min=TBD. External 1M feedback not required (internal 5Mohm nominal used).

**RTC NOTE**: The VDDRTC pin MUST be bypassed with 2.2uF minimum for successful operation.

### 4.2.1. External RTC Drive

If a stable RTC clock can be supplied during startup, then the recommended drive level is into RIN pin is:

(This assumes the elimination of the RTC crystal, and the associated capacitors)

Frequency in =32.768kHz.

Stability =20ppm DeltaF/F or better (less).

Vin = 0 to 1.25V min, 0 to 1.6V max. 40% to 60 % duty cycle. No blocking cap is required. Direct couple to RIN if CMOS driver is used.

VDDRTC power must always be on and stable before any external clock is supplied.

### 4.2.2. RTC crystal requirements

The parameters of the RTC crystal used should be as follows:

Nominal Values Noted.

Rs =80k. Max =TBD

C1 =3.3fF

Cload=10pF

Max drive capability of 0.5uW is suggested.

Alternate values of:

Rs=90k ohms

C1 =2.2fF

Cload=10pF

Are presently under investigation.

The maximum frequency tolerance allowed is +/-20 ppm, deltaF/F.

Nominal frequency is 32.768kHz with a 180k series drive resistor, and 33pF to ground on this node. The RIN node shall have 18pF to ground. This helps to stabilize the "pull-ability" of the crystal, and the offset ratio tends to help improve the start-up time.

Please note that compact routing of this circuit is highly recommended. The trace capacitance should be as low as possible, and all routing should be well isolated from noisy and high speed lines.

Round can packages are not recommended. SMT packages allow for higher success during reflow and over production volumes.

## 4.3. Battery Backed Operation for the RTC Cell and Low Hibernation Currents

It is important to note the limitations of the GSP3f chip for low STAND-BY and HIBERNATE currents. Because this is 0.13um technology, the leakage currents are higher, and the ability to integrate a low quiescent current 1.5V RTC regulator into the chip is not possible. The small process technology limits the internal core regulators quiescent current to be in the several hundred uA range.

It is important that customers be aware that an isolation bit in the RTC registers will be set prior to any shutdown into HIBERNATE. This is done with the latest version of software. This will avoid higher levels of leakage currents that could occur. In addition, ALL EXTERNAL SIGNALS are assumed to be disabled, or held low during any long term sleep or 'HIBERNATE' states. Otherwise, poor leakage currents will occur, since our input pins are not failsafe. Inadvertent removal of IO power without setting the isolation bits is ok, if external drive lines are disabled. If the isolation bit is not set, due to inadvertent removal of power, users can expect much higher VDDRTC leakage currents.

When in HIBERNATE, the code picks up from the last know state for faster wakeup operation. The power is always supplied to the input of baseband LDO, and hence the startup is much quicker than would be for a standard startup state. In addition, the need for an nSRESET low pulse of several hundred ms is not required.

Because of the higher quiescent current of the internal regulators, the need to utilize an ultra low quiescent current, *external* 1.5V regulator is recommended for lowest HIBERNATE currents. This can also be integrated with external, low leakage Schottky diodes in an OR'ing circuit that allows the VDDRTC to seamlessly transition back and forth between the main supply and battery backup. The operation of this chip set is to ALWAYS have VDDRTC voltage present and properly backed up. Failure to implement this into your design may result in unspecified behavior. Be advised that certain regulators may incur a poor transient response during backup battery transition. Any transient glitch at VDDRTC should be less than ~20mV (TBD) to avoid odd RTC clock counting.

It is important to note that use of a backup battery will always involve some type of long term, self discharge characteristic. If the VDDRTC supply potential drops below 1.2V, there is a risk that the BBRAM contents may be corrupted, and RTC clocks stop.

SiRF's software uses checksums on data elements stored in the BBRAM, but designers should take care to protect their data as well.

The use of low voltage detect circuits can provide extra security against using any corrupted values, but is less of a concern with the SSIII RTC cell.

The BBSRAM is arranged in 1024x32 cells, and is selectable with provisions for byte lane control, allowing byte, half-word and word access.

### 4.4. ECLK Input Characteristics

For future reference, the need to supply ECLK with an external reference could be a desirable option. Normally, this is a standard CMOS input of 0 to 2.8V typical swing. The range of allowable input high swings should be greater than ~70% of VDD, and is 3.3V tolerant as a maximum. For booting, the allowable range of input frequencies is 10kHz to 50MHz.

Since the ARM clock is dual edge clocked, it is important to drive this pin with a symmetrical, ~50% duty cycle clock source for initial booting. This symmetry requirement is more critical as the ARM clocking frequency approaches 50MHz. For initial boot frequencies at <25MHz, an estimated safe duty cycle range to assume is between 40% and 60%, since an initial div by 4 is used. Higher boot frequencies should approach 50%. Driving the ECLK input directly with a 1200 mV pp (min.) clipped sinewave at lower frequencies, and a properly centered voltage divider is NOT recommended at this point in time. An external buffer in active bias mode (to square the signal up) is suggested to reduce any design uncertainties when driving ECLK with a somewhat sinusoidal source. Use of single gate AU04 (or similar) type inverter configured in active bias mode will avoid the risk of very low frequency oscillations that can occur with other inverter designs having more than one gate stage per inverter.

If baseband power to the GSP3f is removed such as during HIBERNATE, it is assumed that ANY external drive to the ECLK pin will be disabled, or held low. This is normal design practice. Note: This input pin is not a failsafe pin.

**For SLC3 code**: The ECLK input is also the input pin for **clock correction** used in SLC3.x. The maximum allowable input frequency for clock correction purposes is ~33MHz. Any jitter s/b <+/-500ps on the rising/falling edges this CMOS input. (This implies that any buffer used to drive this pin, be free of excessive noise. Characterization is recommended to verify the jitter level that could occur.) The frequency of this input should preferably be a non integer relationship to the input reference signal at XTALIN. For example, a 26MHz XTALIN frequency, and a 13.0MHz ECLK is a ratio of 2.0. This is not desirable for optimal performance. Ratios like 1.25000, 1.33333, 2.111111, etc, are also NOT desirable. Ratios like 1.25364773 or 2.06593225 etc. are preferred.

Please refer to APNT3014, SiRFLoc Aiding Considerations to better understand the ECLK stability requirements and estimated clock error information needed to support fast TTFF and low C/No acquisition values desired by so many customers. It is **VERY** important to understand and know the estimated ***levels of drift*** (in ppb/sec) for this reference source, on a continuous basis in order to be able to acquire, integrate and track the ultra low signals below -155dBm (~15dB-Hz).

## 4.5. JTAG Requirements and Considerations

**All layouts should allow for some type of JTAG access for system de-bugging possibilities.** Dedicated Test Points is the preferred approach.

If this is not possible, allowing for the use of pull up and pull down resistor as access points is acceptable.

JTMS, nJTRST must have 10k pull up resistors. nJTRST must also follow (or be tied to) nSRESET line during the system reset. JTDO is an output, and can float.

JTDI and JTCK define the operational clock source configuration; therefore refer to **Figure 3.2** and **Table 4.0** again for the desired pull up/down frequency selection and boot configurations.

For Multi-ICE testing, the JTDI and JTCK latch registers must be overwritten in order to bring up the chip on Multi-ICE. Pull up/down resistors are highly suggested to assist in module troubleshooting that can be expected.

### 4.5.1. Special JTAG Test Concerns to Remember

The ARM used in the latest Rev E version of the GSP3f chip has somewhat incompatible HW and SW breakpoints, and is not always repeatable. Please refer to the SDK manual for a workaround solution for this issue.

## 4.6. External interrupts and nEITx considerations

### 4.6.1. ON_OFF Characteristics

- ON_OFF is designed to be a DIRECT hardware connection to the internal state machine. Activation of this pin is intended to 'wake up' the receiver from a STANDBY state or HIBERNATE (extreme low power) state *only*. To properly implement this when in STANDBY, will require monitoring of the RF supply voltage (level) with an external processors' GPIO pin. For HIBERNATE, RFPWRUP and nWAKEUP must be monitored.
- ON_OFF should NEVER be used to shut the chip down! In-advertent triggering of this pin while in the fully powered state will cause the chip to crash. There must be an orderly shutdown procedure to properly configuring the isolation register bits. Implementing this monitoring function will also correctly store the BBRAM contents.
- *When in HIBERNATE mode*, the controlling code must verify that APM is enabled, and verify that all sessions are closed. Note: The controlling code must also allow for a 1 second delay after session is closed, before any attempt to externally awaken the receiver. Refer to the SDK Users Manual for more information. This pin feature for HIBERNATE can ONLY be used with SLC3.1 code and higher.
- If the chip has been externally awakened using the ON_OFF pin, communication activity must occur within 5 seconds, otherwise, the chip will go back into the sleep mode (this applies to STAND-BY only).
- Since it is a direct link to the core, the use of 3.3V tolerant cells was used in the design of this pin. A 0 to 2.8V CMOS signal is preferred, and is designed to be rising edge triggered, and must stay high a MINIMUM of one full clock cycles of the RTC clock, or ~31us. Use of 2 clock cycles, or 62us minimum allows for a degree of safety margin in the timing budget. This is not a fail safe pin. The 1.5V VDDRTC power should always be on and stable before the signal is asserted. Operation without VDDRTC power is only possible with time aiding. It is still recommended to retain an RTC clock, since network availability is not always possible.
- For GSW3 Autonomous operation, it is suggested to pull the ON_OFF pin low with a 0 ohm resistor, since interrupts, and HIBERNATE modes are not supported with this code.

- For SLC3 aided operation, external wakeups are supported; and this pin should be pulled low with a 4.7k to ~10k resistor, depending on the drive capability of the external driving source. Each rising edge of ON_OFF advances the state machine, and awakens the receiver. But, as noted above, if incorrectly implemented, this can shut off the receiver when not desired, and lock it up.
- The best way to avoid the lock up concern is to use a GPIO from the external controller, and monitor the voltage level of the VCC_RF (if low, OK to wake up from the STAND-BY state). This way, a built in system of checks can be implemented in controlling S/W to only enable the ON_OFF pin when the receiver is in the STAND-BY state. A special external gate may be required for some customer applications. More information on this feature will be supplied in the future.
- If ephemeris is more than 2 hours old, the SLC will request new ephemeris upon wakeup from the network. If the network input is not available, and signal strength is strong enough, the receiver will attempt to automatically collect it from the available satellites.

### 4.6.2. nEIT[0]

Interrupts can be handled via the EIT pin.

Normally, the user will hold nEIT[0] low until the interrupt is acknowledged by the interrupt handler, and data can be transferred via GPIO pins, or the serial ports.

For GSW3 code, this pin is available for customers to implement an external interrupt WHILE THE RECEIVER IS IN FULL POWER OPERATION ONLY. No wakeup from a HIBERNATE state is possible.

This will require custom software generated (typically by the OEM) with the SiRF SDK Development kit. The pin defaults to active low, and can be configured to be active high via bit 21 of the ASIC_EIT_LEVEL register. This is a level triggered signal. It has no internal pullup or pulldown, but most customers will choose to tie high with 100k ohms, and drive with an external source.

In general, this pin is powered from the core voltage (not the RTC), so shutdown of any power to the core will disable this function.

It is also 3.3V tolerant, and could withstand 5V for very short periods. The pulse width is 15ms minimum (TBD).

***For SLC3 code, this pin is not implemented. Pull high with 0 ohm or 100k***

For more information, please refer to the SiRFstarIII SDK Software Reference Manual.

## 4.7. SPI ports and interface considerations

The GSP3f chip has a muxed SPI port, and is controlled by the two chip select nSS[0] and nSS[1] control pins. At this writing, the SPI port is not available to users. It cannot be used as an alternate UART port, or a comm port. The SPI is a master configuration only, and not able to be configured as a slave. The high degree of multiplexing and interrupts on this pin, and the use of the SPI for RF chip power management control severely limit the use of SPI outside interface with the GSP3f. For reference purposes, the maximum clock speed allowed is ACQCLK/4 or 4MHz at ambient, and nSS[0] is used for RFIC programming, and is not intended for any external use. This becomes evident when one realizes that the SPI ports of the RF chips are not tri-stated after programming, so sharing is not possible.

## 4.8. UARTS

There are two UARTS available in the GSP3f, designated as UARTA and UARTB.

In GSW3 Autonomous applications, UARTA and UARTB port CANNOT output the same protocol. For example, if UARTA supports NMEA, then UARTB must be set to support SiRF Binary, RTCM or some other user defined protocol. The non standard protocol support capability will occur in later code releases.

In SLC3 aided applications, UARTA uses a channel scheme, and can support any and ALL protocols, while UARTB supports standard SiRF binary or NMEA. Max baud rate is limited to 115kb/sec with this code.

The use of 12 pF output shunt caps is suggested, but not mandatory until further EMI tests are complete. Internal 100k pull-ups are present on the TXA and TXB outputs.

If UARTA is used in an RS485 application, RTS is the output, and CTS is an input.

In future code releases, baud rates approaching 1Mb/sec are possible for flashing only

NEMA MESSAGING COMMENTS:
Can I send NMEA for my application while sending SiRFLoc F/AI3 messages to set various setups?
What are the limitations?
A: There are at present, 8 logical channels that a user can open. All of these correspond to the available protocols in the system.
The user will have to open a logical channel to obtain the NMEA. They will also have to strip the SL wrapper before trying to use it with a NMEA piece of equipment. There is one limitation to observe; when operating with multiple logical channels the software will purposely drop non SL message to ensure that all SL message are received/transmitted properly. Refer to the SDK Users Manual for more information.

## 4.9. Internally Packaged Flash Considerations

The internal Flash chip is limited to 4Mbits of memory in a 512kx8 configuration.

The minimum allowable voltage for this chip is 2.7V.

For GSW3 applications, sufficient unused Flash memory exists for outside applications, perhaps 1Mbit (TBD). Adding external flash is possible.

For SLC3 applications, NO FLASH ACCESS IS AVAILABLE FOR USERS.

For proper flashing, use of SiRFlash v2.14 minimum is required.

## 4.10. Pre-Flashing of the Internal Flash

If desired, it is possible to pre-flash the GSP3f chip before assembly operations. This would require a special socket to secure the part, and gain access to the proper CS pins, and ADDRESS/DATA lines. To pre-flash, insert device into socket, apply power, and tie TMODE high to tri state the output pins. (Note: this pin is normally low, or grounded). Then, proceed with standard flash procedures.
Alternately, use of a USB to serial converter, working in conjunction with SiRFlash 2.14 or higher could also be used for flashing at higher baud rates.

## 4.11. Interfacing to External Memory

The GSP3f chip will no longer support 8 bit or 32bit external memory. So use of MUL[0] and MUL[1] is no longer available. The only memory that can be supported is standard 16bit memory.
For this situation the suggested SRAM memory connections should be: pull LB and UB pins low. Then, for any 8-bit access, simply operate on the desired byte. If the user has to have an array of 8-bit values, then a read-modify-write cycle could work (read the existing 16-bit value that contains the desired byte, mask off the byte to change and change it, then rewrite the modified value, changing only the desired byte). This effort may take a bit more code, and may slow down the writing process, but the read will be essentially the same speed, with only the byte extraction process added. The writes can be the same speed if you operate on 2 bytes at a time in appropriate situations.
A sample connection diagram for 16M FLASH and 32M FLASH is shown in Appendix B.

Note: ED7 is different than previous generation chips, and must now be pulled LOW for this chipset when interfacing to 16 bit memory.

## 4.12. Interfacing to External Flash or SRAM

Addition of an external 10k pull-up to VDD on pin G10 (nCS1) of the 3f will be required. This will avoid any 'back-drive' conditions during reset, and is only needed w/external memory.
Customers must realize that there are 2 banks of 16 wide memory, and nCS1 fires the first half of the flash at 41million, and nCS2 fires the second half of the flash at 42 million, so THERE EXISTS A DISCONTINUOUS BOUNDARY to be aware of. This gap in memory could be over 500k, but is compensatable if the proper memory alias is addressed, and the proper bits of the chip select registers are configured. Please refer to the SDK Users Manual for more information.

## 4.13. Other Functions (and pins)

[Please refer to **APPENDIX C** for a cross referenced list of all GSP3f pin functions]

**AGCPWM** (multiple use pin: Also noted as GPIO[2]) The typical pulse width is ~11,700ns (bits 11111) at the lowest IF gain, and ~367ns wide (bits 00000) at the highest IF gain. The repetition rate is 1000Hz.

**nCS[x] Chip Select Considerations:**

**nCS[0]** This is the primary external bus chip select pin. The valid address range always starts at address 0x40000000. Has internal pull-up of 100k.

**nCS[1]** (multiple use pin: Also noted as GPIO13, nCTS)

May be used for additional memory devices. The address range is set by chip select registers which also set the read/write characteristics. NOTE: This pin DOES NOT have an internal pullup. An external P/U may be required for external memory due to the flow control in this pin.

**nCS[2]** (multiple use pin: Also noted as GPIO14, nRTS)

May be used for additional memory devices. The address range is set by chip select registers which also set the read/write characteristics. Has internal pull-up of 100k.

**nCS[3]** (multiple use pin: Also noted as GPIO15, YCLK, **TIMERSYNC**)

May be used for additional memory devices. The address range is set by chip select registers which also set the read/write characteristics. Has internal P/U of 100k. Supply the rising edge signal for time aiding to this pin.

**ED[0:15].** ED[0:15] Memory data lines: Some of these pins are configuration straps that use external pull ups or downs to set internal registers during the reset process.

**GPIO[0]** (multiple use pin: Also noted as REVERSE)

This pin controls an external Darlington transistor switch (UMC3N), which enables power to the external LNA used in the SiRFStarIII design.

Further discussion of power management and related operation and concerns is discussed in the RF front end operation below, and also in APNT3008, Advanced Power Management Considerations.

**GPIO[1]/ODOMETER:** The odometer function is basically a placeholder for future use and evaluation. This block will count rising edges at the ODO pin. The function requires that the high period of the ODO signal be a minimum of one µs long and that the frequency of the clock provided by the clock control block be at least three MHz.

**GPIO COMMENTS:** For GPIO values, port direction and port value assignments for the multi-function GPIO pins, refer to the APNT3005 GPIO Pin Functionality for the SiRFSstar III, or the SiRFstar III SDK Users Guide.

**nMWE** External memory write enable**.** Active low.

**nMOE** External memory output enable. Active low.

**MUL[0]** This is the lower external 16 bit memory byte select access (lines 0-7). The GSP3f NO LONGER ALLOWS for this control in the present package.

**MUL[1]** This is the upper external 16 bit memory byte select access (lines 8-15). The GSP3f NO LONGER ALLOWS for this option in the present package.

***NOTE: SiRFStar III will only support 16 bit interface in little Endian format only. Pull D7 low for 16bit interface. Special code needed to perform word masking if byte transfer is needed. See the SiRFStar III SDK manual for register address and control information.***

**PLL_FILTER** This pin should by bypassed with a nominal 0.01uF capacitor to ground. Use of X7R capacitor material is preferred.

**nRESET** This pin may be used for control of external ICs as well. It can be used to reset the GRF3 SPI block on power up, since nRESET "echos" or follows the nSRESET state (with a slight propagation delay). It is also used to reset the GRF3w logic after power has been removed from the part using nWAKEUP or RFPWRUP to control the corresponding regulator enable pin. nRESET can also be used to control the outputs on an external flash memory that continues to be powered during power down operations. It can control the output state of an external RAM that continues to be powered during power down states, as may be the case for applications requiring additional non-volatile RAM.

Internally, this is an open drain, so an external pullup (recommended value: 10 kΩ) is required for proper operation. The open-drain circuit can tolerate up to 3.6 V pullup voltage, but the GRF3w can only tolerate 3.0 V, so we recommend that you limit the voltage on the pullup to VDDRF or 3.0 V, whichever is lower..

**nSRESET** This is the primary system reset for the ARM and internal core. Active low. nJTRST (JTAG reset input) must also be tied to this pin. **Once system boot clocks have stabilized**, hold low for a minimum of 40 clock cycles. The external power on reset generator (POR) circuit supply and the output pullup must be tied to an always present power source. Internal flash does not need a nSRESET connection. ***Therefore, do not tie this to the VDDBB if Advanced Power Management or hibernation is used.***

**RFPWRUP** (multiple use pin: Also noted as **GPIO[8])** This is an active high output, and enables the regulator that powers the GRF3w and is used for power control of the RFIC. Since the RF chip requires SPI programming, power is enabled first, before programming can occur. The default output is high at reset, connected to and controlled by the Finite State Machine.

When configured as a GPIO, the only available functions are output and high impedance; there is no input function available on this pin. This pin does not have a pullup or pulldown resistor internally – any desired pullup or pulldown resistor must be supplied externally.

**SCLK** This output is for external synchronous memory, and can output the system clock up to 50MHz for monitoring purposes at CMOS levels. Typically, this will include 7 wait states, depending on the version of code. This is also an available output port that can supply a divided ECLK or BCLK output (BCLK is the ARM clock). The max divider ration can be programmed to $2^{16}$-1 Test point access is highly recommended during layout.

**SIGN_MAG** The SIGN_MAG input pin allows for special demuxing of a serial and combined SIGN and MAG serial data stream in future designs. In the situation of use with the GRF3w, the SIGN output connects with SIGN_MAG input of the GSP3f, and the MAG output of the GRF3w connects to GPIO[4] input of the GSP3f. Test point access for these signals **is highly recommended**.

**SI** SPI INPUT data pin The SPI interface with the GRF3w is unidirectional and therefore the SPI input signal is not available to use. Also a GPIO function.

**SO** SPI OUTPUT data pin. Also a GPIO function.

**SK** SPI CLOCK pin. Also a GPIO function.

**TIMEMARK** (multiple use pin: Also noted as **GPIO[9]**)

This pin provides the 1pps output desired for certain applications. This is a CMOS level output. This function is available with an approximate accuracy of +/- 35ns, but could be as high as +-100ns over all conditions and temperatures. The rising edge is synched to the GPS Epoch.

**TIMERSYNC** (multiple use pin: Also noted as nCS3, GPIO[15], YCLK)

This pin is used for time transfer information into the SiRRstarIII receiver with SLC3 code ONLY, and also for alternate applications. When use as a TIMERSYNC input, this input pulse is rising edge triggered, and must be 123ns wide as a minimum, and 1ms wide as an approximate maximum.

**TMODE** This pin must always be pulled low or shorted to gnd. It is used for special factory ATE testing.

**INTERNAL FLASH:** The internally packaged Flash is a SST 39VF400A part, and is arranged in a 256x16 configuration.

### 4.14. Watchdog Timer Function

The watchdog timer provides a mechanism to detect and recover from unexpected software or system behavior. The watchdog operates by requiring SW to periodically acknowledge an interrupt. If the acknowledgement does not occur, the watchdog self-times out, and initiates a S/W system reset. A flag set in the watchdog registers allows SW to know that

the reset was caused by the watchdog, so that appropriate recovery or notification of the event can be attempted. More information can be found in the SDK Users Guide.

### 4.15. Special Advanced Power Management (APM) Considerations and Control Pins

**nWAKEUP**: As previously noted, this output pin must be pulled up via a 100k resistor, **to an always present and continuously "on" or non switched voltage source!** Do not tie this pin to the regulated BB power. The pull-up supply voltage must never exceed 3.6V, including transients. The maximum allowable sink current for this pin is 1mA over temperature.

For proper isolation of the chip circuitry, the software configurable isolation bits in the RTC control register (0x80040018) MUST be enabled first, before the chip is put into any long term sleep or hibernate mode. In addition, if placing the GSP3f chip into a long term hibernate state, it is initially suggested that any driving I/O from outside sources or processors be disabled, or preset to a low state. This includes ECLK, TIMERSYNC, RXx, TIMEMARK (in certain situations) and other GPIOs if special S/W is implemented. Inadvertent removal of power could induce odd leakage characteristics if external drive is not disabled. Retaining power to nWAKEUP, nRESET and VDDRTC is acceptable.

### 4.16. Interfacing to the RF chip

A primary concern when interfacing the RF front end outputs to the GSP3f baseband processor is signal integrity and noise.

For EMI purposes and current consumption reasons, the drivers for the RF chip are not high current drivers. If an end user desires to run the outputs of the RF chip (SIGN, MAG, CLKACQ, AGCPWM) through a high density connector, and with long trace runs, then problems can (and will) be anticipated.

SiRF suggests that the interconnect length for these CMOS buffers be kept under 1 inch, (2.5cm) when possible. **Running these signals through a connector is NOT recommended**, unless proper characterization is performed in advance of initial layout.

Use of source termination resistors may help to improve the ringing that can be associated with CMOS drivers. Therefore, adding 27 to 33 (TBD) ohm series resistors within 5mm of the OUTPUTS of the RF chip will usually improve the driving source characteristics, assuming a 50 ohm trace is used. Allowing for these resistors is HIGHLY recommended for probing and test access, when needed. These resistors could always be replaced with 0 ohm resistors if needed. If no resistors are used, adequate test access to these lines should always be allowed.

All clock lines, and high speed lines, should always have a minimum of three trace widths separation between potential offending lines. Adding a well grounded isolation trace between these traces will also help with noise reduction. Additional suggestions can be found in APNT3002, PCB Design Guidelines for SiRFstar III Implementation.

Since many of the pins are dual use, it is important to realize that the RF chip SIGN output will go into the GSP3f SIGN_MAG input. The MAG output of the RF chip will go into the nSS[1]/GPIO[4] input pin when the GRF3w is used. AGCPWM (also noted as GPIO[2] will be used to drive the AGC control for the IF section.

## 4.17. GRF3w RF Front End Operation and Interface Considerations

### 4.17.1. Power supply requirements, and initial power up considerations for the GRF3w

The GRF3w is designed for 2.7V to 3.0V operation. Current consumption in full power mode, with the LNA and TCXO can be expected to average about ~33mA [TBD] at 2.85V. This is the preferred operating voltage for the GRF3w chip. This is also the preferred voltage for the TCXO. The ripple and noise requirements should be as low as possible, since the TCXO typically runs off the RF supply. Power supply noise and ripple from DC to 3MHz is still TBD, but a safe value to strive for would <40uV max. The lowest noise possible, the better. If TCXO power is shared with the GRF3w, it is important to choose a regulator with ~1mV voltage change per degree C for best, low level sensitivity while in a thermally dynamic environment.

The GRF3w is a SiGe chip with extremely high gain. Integrated into this chip is a fractional N synthesizer that allows the user extreme versatility in the choice of reference clock that could be used. The chip is packaged in a 5x5mm QFN32 package. See Appendix A for the suggested solder pad footprint.

This RF chip was originally designed for a standard default reference clock frequency of 16.800MHz, and was designed for SiRFstar II and III applications. If a user selects this frequency, the chip will power up and synthesize the necessary 16.369MHz output out of the fractional N synthesizer after the Fractional-N re-conversion, but with PECL output drivers enabled. Therefore, SPI re-programming will still be required to reconfigure to CMOS output drivers.

Since this chip is SiGe, it is extremely important to not exceed the absolute maximum voltage requirements for this part, which is 3.15V. SiRF does not recommend operation above 3.0V.

The maximum allowable VDDBB to VCCRF interface voltage difference is 0.25 (TBD) VDC.

**NOTE: Use of ESD protective garments and adhering to strict ESD handling procedures is highly recommended when working with these parts.**

**In addition, advance planning of HBM ESD related concerns MUST be properly considered and addressed for those customers that have risk areas. The weak areas of ESD sensitivity are SAW filters, RF inputs; LNA's and associated RF sections.**

## 4.18. RF Considerations with the 3w chip

### 4.18.1. Internal vs. External LNA in the GRF3w, Filtering and Antennas.

Although the GRF3w does contain an integrated LNA, SiRF has chosen not to use this in any reference designs. The performance of this chip function is not as advantageous as what can be achieved with an external LNA. An external LNA will offer much superior performance.

Many customers ask about RF front end design: When do we need an LNA? What type of LNA? Do I need a prefilter? What kind of post filters should be used?

These questions are common, and the following rule of thumb should apply:

a) A GOOD antenna and LNA will ALWAYS be required to achieve the desired performance. The antenna and the TCXO are the most critical items for successful GPS reception in a weak signal environment. Proper choice and placement of the antenna will ensure that satellites at all elevations can be seen, and therefore, accurate fix measurements are obtained. Most customers contract with antenna design houses to properly measure the radiation pattern of the final mounted configuration in a plastic housing with associated components near the antenna. Linear antennas are becoming more popular, and the gain is reasonable, since a smaller ground plane can be used. Choose a linear antenna with a reasonably uniform hemispherical gain pattern of >-4dBi. Use of an antenna with lower gain than this will give less than desirable results. Please note that a RHCP antenna with a gain of -3dBic, equates to the same gain achieved with a linear polarized antenna of -0dBi.
   Proper ground plane sizing is a critical consideration for small GPS antennas. Therefore, proper placement of the GPS antenna and TCXO should always be the FIRST considerations in integrating a GPS layout. The best implementation possible occurs with proper antenna planning!
b) Prefilter: If the unit is a stand-alone receiver, with minimal outside interference, and the typical operating environment is free of harmonics and spurious energy in the 1575.42 MHz +/-6MHz band, then a prefilter is not suggested. It will degrade the overall noise figure, adds to the cost, and complicates the front end matching. If integrating into a handset, or multiple radio devices, the use of a prefilter is suggested for best performance. Extreme care must be exercised in the choice of the prefilter used. If this is a SAW device, mismatch effects will increase the insertion loss, and add to the front end noise figure. Close attention to source and load matching is very important, since poor source and load return loss will increase the filter insertion loss, and degrade the amount of rejection possible. Periodic sampling of production lots to validate matching in high volume production is suggested.
c) The post filter will offer the best rejection opportunity before the signal goes thru the necessary signal processing. The higher the ultimate rejection, the

better the anticipated performance. A SAW with an insertion loss of <2.4dB and rejection of >=38dB at +/- 75MHz offset is the minimum suggested rejection. The higher the rejection, the higher the probability of mitigating any potential interference problems. A good rejection peak at 1650MHz also helps in rejecting any PA harmonics. Once again, good source and load matching provides for a more repeatable SAW insertion loss, and rejection characteristic. If the gain of the LNA is high enough, use of a resistive -2dB or -3dB pad after the post filter and before RFIN is a good position, and will help to improve the matching concerns.

d) The Fractional N loop filter BW is slightly greater than 100kHz.

### 4.18.2. Allowable LNA gain range and characteristics for the GRF3w part

SiRF recommends that the range of TOTAL LNA gain before the RFIN pin of the GRF3w be between the ranges of **12.0dB minimum and 26.0dB as a maximum.** This estimate includes all cable and filters losses, and assumes an antenna with gain of 0dB+/-approximately 3dB. In past designs, some customers chose to implement an external active antenna, in front of the primary and integrated LNA. This could occur, but SiRF does NOT recommend this approach. It will not improve the sensitivity of the total receiver chain. If an improvement is observed, it is most likely due to the improved antenna gain characteristics that can be obtained with an external antenna. Adding this extra gain will cause overdrive issues in the IF section and the quantizers, resulting in reduced quantizer performance. It can also contribute to significantly reduce jamming resistance in the presence of an in-band, or near band interferer, depending on the gain characteristics of the active antenna and subsequent RF chain.

The LNA noise figure should be as low as possible (target <1.5dB) but slightly higher noise figures are allowed if the input and output return loss characteristics of the LNA are better than 15dB. This will help to improve filter characteristics, and reduce total mismatch loss. Use of high Q (>50 or 60) inductors on the series input matching is always suggested. Lower Q (<20) inductors on the output may help to improve output matching. Use inductors and matching caps with 2% tolerances for enhanced unit to unit repeatability.

A suggested example schematic of an external active antenna connection node to bypass the internal LNA is shown in Figure 5 below. The use of an optional pi pad can help the amplifier stability, and SAW filter response characteristics. This assumes the amplifier has a gain of at least 17dB for a -2dB pad, or 18dB for a -3dB pad. Ideally, the RF power must be disabled to the LNA not in use.

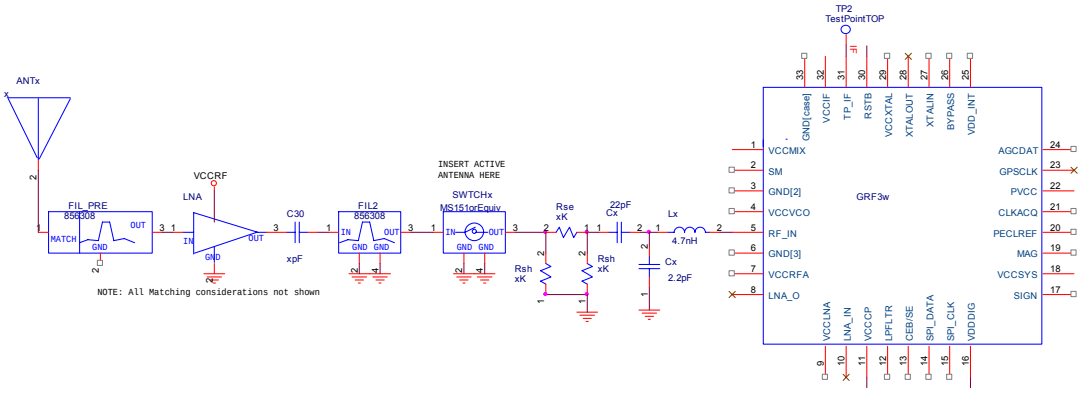



**FIGURE 5: Active Antenna Injection Point**

The LNA -1dB compression point should be as high as possible, especially in a highly integrated handset platform. Unfortunately, the higher current draw associated with a higher P1dB LNA is not desirable for battery life. So, compromises can be expected to occur. Usually, a -1dBout compression point of 0dBm can be adequate, if proper PA notch filtering and good isolation techniques are implemented.

Extreme caution should be exercised in the layout of a GPS LNA section, since the probability of oscillations anywhere from ~100kHz to 11GHz can exist. All finished RF layouts should be totally scrutinized for stable operation under all source and load conditions up to 12 GHz minimum.

## 4.19. TCXO Considerations (ALL SiRFstar III designs)

The TCXO requirement for SiRFstar III chipset are considerably much more demanding than previous generation receiver requirements and is discussed below.

When acquiring and tracking deep space satellite signals at very weak levels, oscillator stability is extremely CRITICAL! This cannot be emphasized enough.

Choosing an inexpensive TCXO with this receiver is comparable to running a high performance race car with diesel fuel. The desired results will NOT be obtained.

SiRF recommends (at a minimum) the use of a 0.5ppm temperature stability TCXO that meets all the requirements noted in the SiRF document: GPS Clock Specification for the SSIII System, July 2004 or later.

There are many parameters that are critical requirements that must be met. Phase noise, frequency ramping, thermal gradients, aging, g-sensitivity, frequency micro-jumps, etc., can all affect the ultra low signal acquisition and tracking performance of this deep space receiver. If you are unfamiliar with these requirements, contact your SiRF representative for a copy of this document if you require a more detailed understanding.

**TCXO NOTE:** Use of a crystal for an oscillator is not recommended, nor is it a cost effective option. The desired low signal sensitivity will not be achieved unless the proper TCXO is used.

It is also extremely important to plan well in advance the proper placement of the TCXO for the lowest exposure to thermal gradient and ramping situations. The primary cause of poor performance in a highly integrated GPS receiver is thermal ramping of the quartz blank inside the TCXO. SiRF recommends that any heat source such as an IC or regulator be located far away from the TCXO. In addition, the use of a cover for the TCXO is also highly recommended for best performance. An excessive thermal ramp rate of tens of milli-degrees per second can cause tracking problems. Smaller TCXO's appear to exhibit a higher degree of sensitivity to thermal transients, due to the ultra low thermal mass that these parts exhibit. Use of ultra small TCXO's should be fully characterized before design implementation.

The power supply voltage for the TCXO should also be extremely quiet and stable over the full temperature range. Supply voltage deviations of +/- 0.5% from -40C to 85C should be considered the approximate maximum allowable change allowed! A 0.3ppm over the -20C to 70C range is suggested. Most TCXO's are designed for proper operation with a 2.85V supply, and a stable load of 10k ohms in parallel with 10pF. An alternate terminating load for the TCXO could be 20k ohms in parallel with 5pF. The GRF3w will come close to this value, but the resistive term will vary over temperature and from unit to unit. Although not required, adding an optional 75k resistor in parallel with the XTALIN pin will help to stabilize the impedance of this pin slightly. The input Z of this pin appears as a series combination of ~110 ohms in series with 170nH at 2.85V. The shunt equivalent is much higher.

The use of filters on the output of the TCXO is not mandatory, since a doubler is not used.

The minimum input swing required by the GRF3w is 200mVpp over all temperatures, and the absolute maximum allowed is 1200mV pp with a 1000pF ac coupling cap. Exceeding this can overdrive the linearity of the input, and damage the ESD protection diodes on the input of the chip.

Locating the TCXO in a thermally benign area like behind the keypad is suggested, but careful routing of the TCXO clock to the critical sections will be required, and any noise coupling must be non existent.

**NOTE: Deviation from the recommended TCXO can result in poor, weak signal acquisition or tracking performance. There are many parameters involved that contribute to the high level of frequency stability required by the SiRFstar III chipset. Use of alternate TCXO's or power supplies for the TCXO, not recommended in our reference designs, will require that the customer perform an EXTENSIVE amount of additional testing to validate the TTFF and system sensitivity under various operating conditions in the final integrated product. This also includes the vibration and handling related oscillator stability concerns. This is due to issues such as quartz crystal mounting, design of the compensation ICs inside the TCXO, internal regulation inside of the TCXO, etc. This extra testing should not be viewed a trivial effort!**

## 5. System Operation with Alternate RF Front Ends

This section is left blank for this revision, and will be discussed in more detail in subsequent application notes. Alternate SiRF RF front ends can be used to interface to the GSP3f.

## 6. Weak Signal Acquisition Considerations

It is important to note some general concerns about acquiring weak signals with the SiRFstar III chipset.
For the lowest sensitivities, in the order of 15dB-Hz to 30dB-Hz, longer integration times WILL be required. At present, the SiRFstar III code allows for up to 900ms integration times, and longer shutdown times. In this weak signal mode of operation, position update rates of 2 to 5 seconds is the best that can be expected.
For future releases of Adaptive Trickle Power operating in weak signal environments, the receiver will attempt to acquire satellites up to 6 cycles of ON/ STAND-BY. If no acquisition occurs after the sixth attempt, the receiver defaults to full power operation. The customer is again reminded that minimization of the full power operation can be achieved with the proper planning and placement of a proper GPS antenna. In fact, when integrating the GPS into a handset or PDA, the placement of the GPS system should be given first priority for placement and orientation!

Once satellites are acquired at full power, the power management can continue in tracking mode.
For those users who are not as familiar with GPS receivers, it is important to note that TTFF is a function of probability. The number of satellites in the sky, the position of the satellites, the ephemeris information, frequency errors, noise, multipath errors, etc, all contributes to the variables needed to compute a valid position with an estimated position accuracy. All TTFF tests should be performed and averaged over a 24 hour period for comparison purposes.
SiRFstarIII offers exceptional performance over SiRFstarII TTFF values, especially in areas of coarse aiding operation, and ultra low (<20dBHz) operation.
Please refer to APNT3008 and APNT3014 for more information about SiRFstar III receiver performance in aided and non aided scenarios with and without power management.

## 6.1. SiRFLoc Aiding Considerations

Aiding comes in several forms, and must be properly planned for in advance to obtain the best sensitivity. In the world of GPS receivers, accurate time and frequency correction can mean the difference between a fast, accurate fix, and a slow fix.

1. Time Aiding. This is provided via the TIMERSYNC pin. There are two types of aiding that need to be supplied.

   a. Coarse Time Aiding: This is typically accurate time to within +/- 2 seconds w/o offset.

   b. Precise Time Aiding: This is typically accurate time to within +/-100us, s/b +/-10us.

The difference between the coarse time aiding and fine time aiding will drive the achieved TTFF values, and C/No levels. With coarse 2 second time aiding, only ~23dB-Hz signal extraction is possible.

2. Clock Correction Information: The clock correction is supplied via the ECLK pin. This ECLK signal must be accurate to less than +/-0.1ppm for best low signal results. It is VERY important that this precise reference frequency be free from steering, or outside frequency adjustment while the weak satellite information is being captured. In addition, information about slow drift characteristics (df/dt) of this clock frequency should be sent to our receiver via the SiRF message structure in order to achieve the ultimate low level sensitivity! Failure to supply the needed drift characteristics at a 900ms update rate (SLC3.1) will eliminate the ability to achieve the desired weak signal tracking capabilities.

For weak signal acquisition (~15dB-Hz) and fastest TTFF, it is assumed that the following aiding parameters are present: TCXO frequency error over temp <0.3ppm, Location information is accurate to +-10km, time is <+-10us, velocity is <50m/sec, and no frequency shift dynamics are occurring. Drift, or df/ dt should be <+/-5ppb/sec. The user should refer to APNT 3014 for more information on the various aiding considerations.

# 7. System Integration Considerations into a Handset or PDA

## 7.1. Digital and RF Interface Issues:

Level translation Issues when Interfacing to Supporting chips with 2.5V or 1.8V Interfaces

In general, the primary pins to be used for lower voltage interface with an external processor will be:

RXA or B

TXA or B

ON_OFF (use with SLC3 code only)

nEIT[0] (GSW3 code only)

TIMERSYNC (GPIO[15])

RFPWRUP (Needed to monitor standby or hibernate states)

And possibly RIN

Using the assumption that a 2.85V supply is used for the GSP3f baseband, toggling the ON_OFF, EIT[0], RXA/B or TIMERSYNC pins with a 0 to 2.5V logic level CMOS signal should be acceptable, with acceptable noise margin. Use of drivers with 1.8V swing will most likely require level translators. As noted before, monitoring of the RFPWRUP pin with a 3.3V tolerant GPIO from an external uP should be implemented to avoid inadvertent system shutdown at the wrong time. If a GPIO is available, but is not 3.3V tolerant, then the use of a high value resistive divider (TBD) could be considered, for low current considerations.

Other pins may need to be considered for certain user configuration that cannot be discussed in this application note. Consult with a SiRF applications engineer for additional advance planning if this is a possibility.

## 7.2. SiRFstar III Power Sequencing (in general)

If alternate LDO's or power supplies are in consideration, and are different then the implementation on the reference schematic, then further discussions with a SiRF applications engineer is highly recommended.

If some alternate power arrangement is desired, then in general, RTC power should always be supplied first and is ***always*** assumed to be present.

I/O power should be supplied next, and core power should be supplied after that. The power should be within 90% of normal VDD power within 10ms (TBD) of each other.

Ideally, apply VCCRF at the same time as all VDD core and IO power is applied. If this is not possible, apply VCCRF within 10ms of BB core power being supplied. Since nSRESET is usually a minimum of 100 ms long, then no signals from the baseband should

be applied to the RF chip until nSRESET transitions high. This should allow for safe inter-chip operation.

For customers who want to implement alternative power schemes, please present to the SiRF Applications Engineering team a timing diagram of desired voltages and the desired power sequencing scheme. We also will need to understand the characteristics of these alternative power sources (noise, ripple, turn on time, etc) to see if they exhibit adequate requirements properties to successfully work for the weak signal acquisition.

### 7.3. RF Related Jamming and Test Issues

In-band jamming and Near-Band/Out-of-Band Jamming (What to prepare for).

Additional information regarding this subject can be found in APNT3004: Co-Location and Jamming Considerations for SSIII Integration.

In general, for in-band jamming, the following levels of maximum in band allowable power is suggested for proper acquisition of weak (~<16dBHz) signals:

All CW signals in the 1575.42MHz+/-10MHz band are ideally below -140dBm, but the following breakdown of jamming is expected to be;

a. From +/-0Hz to +/-4.092MHz offsets, any CW jammer s/b below -140dBm
b. From +/-4.093MHz to +/-10.0MHz offsets, any CW jammer s/b <-120dBm.
c. From +/- 10.01MHz to +/-20.0MHz offsets, any CW jammer s/b <-110dBm.
d. From +/- 20.01MHz to +/-50.0MHz offsets, any CW jammer s/b <-100dBm.
i. Outside of this depends on filtering and layout and is still TBD.

(This is why it is critical to plan for proper shielding and isolation of other subsystems!)

GSM PA and Spurious/Noise issues: When integrating the SiRFstar III receiver with a handset or modem that has a high power PA, it is extremely important to add a notch filter on the output of the PA. It is doubtful that proper weak signal acquisition can occur without this filter.

For example, if transmitting at ~835MHz, the second harmonic will be 1670MHz. This second harmonic is at power levels of -50 to -80dBm, depending on the filtering, the PA characteristics, and the isolation possible. Adding a shunt LC filter (in a series resonant configuration at 1575MHz) will reduce the noise power coming from this offender.

A small penalty in PA output power may occur (perhaps 0.2dB), but this filter will be mandatory for ultimate low signal performance.

Another consideration is the backlighting for the LCD display. Most LED backlights are now powered by switching power supplies. It is important to keep any radiated harmonics from this offender out of the GPS band.

Monitoring of the TPIF test point of the 3w (pin 31) with a high impedance RF FET probe or special wide BW, FET input op-amp on a spectrum analyzer can sometimes allow a designer to see if jamming signal are coming into the GPS IF passband and causing interference. See Appendix B for an example schematic of a high impedance ckt. Allow for this troubleshooting option during the layout phase. Special code will be needed to enable this access node. Refer to a SiRF FAE for a copy of HS3_C13_FLASH.s file.

# 8. Layout Comments and EMI Mitigation

The key issues to plan for when implementing a layout for the SiRFstar III receiver:

a) Isolation (via proper shielding and partitioning)
b) Rejection and filtering techniques
c) Elimination of conducted emissions

## 8.1. GSP3f Power Planes, Decoupling and Broadband Noise

1) Plan for solder cover shields over all subsection of the integrated platform, and maximize the radiated and conducted isolation. As mentioned earlier, the TCXO will need the highest isolation from power supply noise, thermal air currents and conducted currents, and low frequency vibration, induced from speaker-phone micro-phonics, and poor mounting configurations that amplify vibration characteristics. Most customers implement this shielding approach with a high degree of diligence and advance planning. Good shielding can help antenna performance too! All designs should always be evaluated and tested under an expected level of vibration and other environmental conditions.

2) Highly integrated receivers with many functions will require multiple board spins in order to achieve the final desired performance. **Plan in advance for this**. It is usually the norm and not the exception due to the high degree of system interaction.

3) Reduction of the switching power supply EMI noise is a concern for the SiRFstar III chipset. Switching noise creates multiple harmonics over a broad frequency spectrum. This noise can be radiated, and fall into the GPS passband at very low signal levels, or the lower frequency energy can be inadvertently coupled into the power supply of the RF/IF section, or the TCXO supply. This will modulate the supply, and show up as a noise spike in the GPS passband. Therefore, the potential of switching harmonics must be well characterized before the design is finalized. Use of higher frequency switchers at 2.0, 3.0 or even 4.0MHz may allow for improved performance, because the noise will be further from the GPS information band. Testing and characterization is a must. Ideally, any SMPS switching should occur at the harmonics of 1.023MHz, with a minor offset. This can be derived from the SCLK output of the GSP3f.

Additional discussions about layout concerns are documented in APNT3002, PCB Design Guidelines for SSIII Implementation.

# 9. Packaging, Assembly and Rework Considerations.

It is important to consider that the GSP3f part is an MSL Class 3 part.
If the part is outside of the protective shipping enclosures for more than 168 hours, the parts must be baked out prior to assembly for a minimum of 24 hours at 85C, or 6 hours at 125C.
It is also HIGHLY recommended to bake out any BGA package for 12 hours minimum (24 preferred) at 85C prior to any attempted rework efforts.

# 10. ESD Ratings

## 10.1. GSP3/f Ratings

The HBM rating for the baseband processor is +-1kV. The CDM rating is +-500V, and the MM rating is +-200V.

# 11. DOCUMENT MAINTENANCE

## 11.1. Required Approval for Changes

Changes to this document require the approval of Hardware Engineering and Field Applications Engineering.

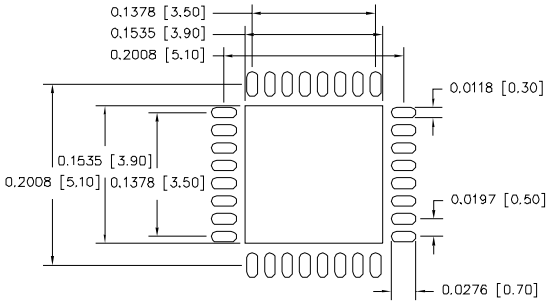
## 11.2. Revision History

| Rev. | Release Date | CN Number | Description | Originator/Editor |
|---|---|---|---|---|
| 1.0 | 2/5/05 | 2675 | Initial Release | JC Chernicky |

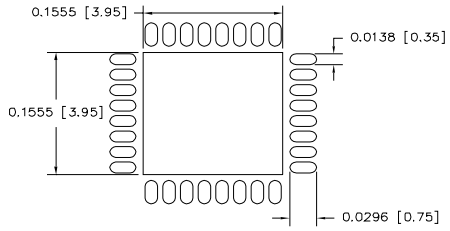
# 12. Appendices

## 12.1. Appendix A – Recommended Solder Pad Footprints

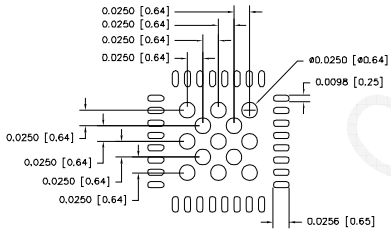
These drawings should allow for a small amount of test probing access to the leadless GRF3w package.



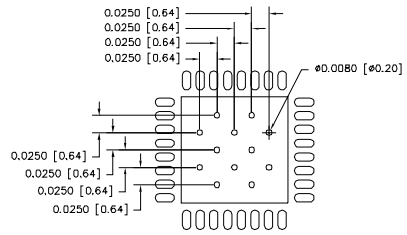

PAD LAYOUT




SOLDER MASK



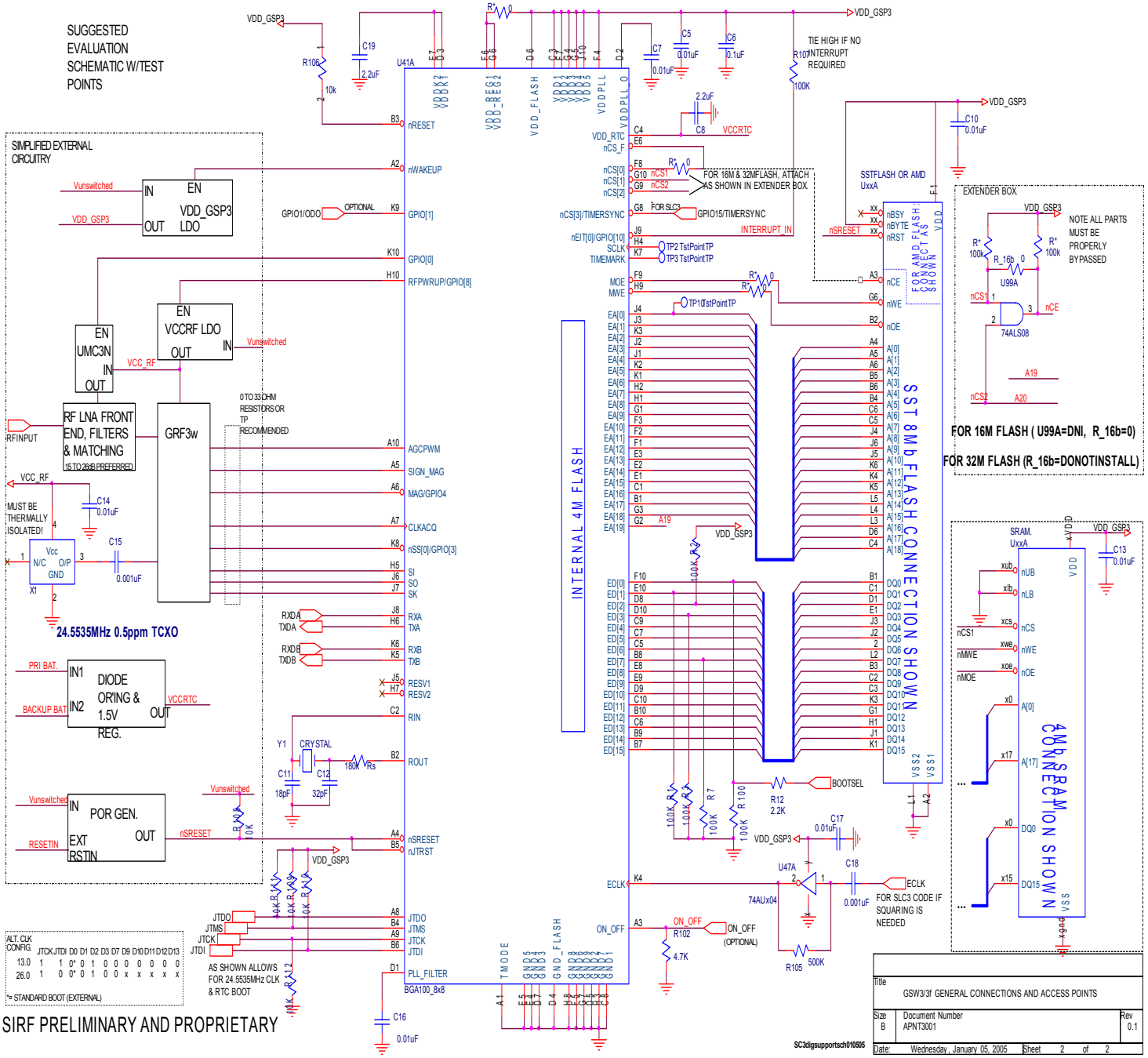

SOLDER PASTE




GND VIA'S

## 12.2. Appendix B1 – External Memory Interconnect Diagram and Test Circuits.

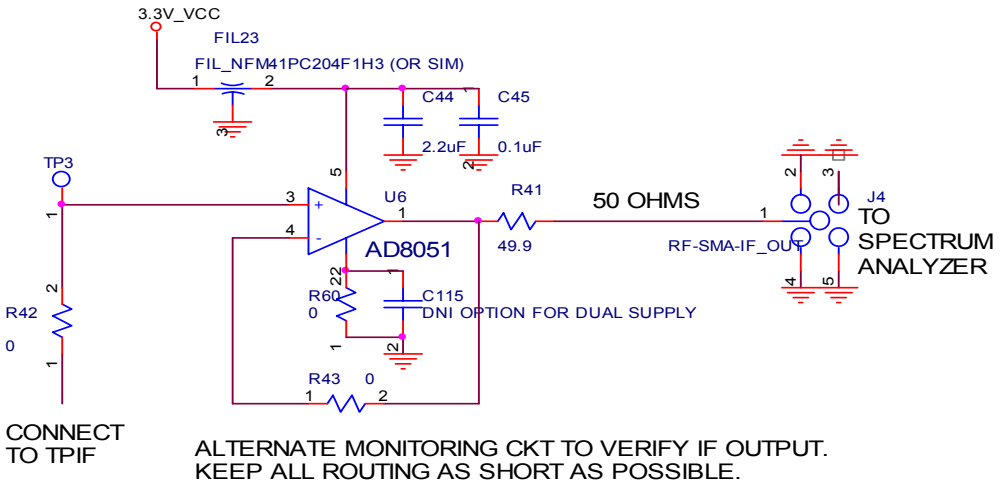
The following schematic is an example of how external SRAM should be connected.




For the external flash address line additions, please be advised, this solution could be potentially risky.
Notice there is no hold time on A20-it can change just ahead to nCE. Customers will need to characterize this approach before production implementation occurs.

## 12.3. Appendix B2: Suggested Buffers For Testing

The following schematic is an example of a test circuit to monitor the TPIF and low frequency characteristics. The -3dB BW is about 90MHz.




For customers who do not have access to an Agilent low phase noise signal generator, we recommend contacting Kyocera or Rakon to obtain higher precision oscillators with clipped sine wave outputs. This higher precision is highly sugggested for substitution testing of the TCXO.

## 12.4. Appendix B3: ECLK Buffer Circuit.

Refer to U47 in the schematic used for section B1. An external switch or mux circuit may also be considered depending on customer application.

## 12.5. Appendix B4: Startup and Flashing Sequences:

**Section I: GSP3f +GRF3w STARTUP AND PROGRAMMING SEQUENCES**

**FOR STANDARD BOOT MODE (RUN FROM EXTERNAL FLASH)**

In general, any problem should always be checked against a known good EVK unit. This is the best way to compare waveforms and signal levels that should be present at certain times.

If an EVK is not available, the following sequence of events should be reviewed and verified for proper behavior.

1. At initial power up, power supplies are switched on, power is supplied to input of the regulators output voltages begins to stabilize, and oscillators start up and begin to stabilize. Verify these waveforms.
2. The Power On Reset (POR) generator senses this ramping voltage, and holds nSRESET low for a ***minimum*** of 200 (TBD)ms while voltages & waveforms stabilize.
3. The ARM processor in the BB will require a minimum of 40 stable clock cycles before operation can properly begin.
4. For the 3f+3w combination, most applications require the RTC clock to be present ***and stable with adequate amplitude (>900mVpp)*** to initiate the ARM operation. Therefore, the customer should verify that the RTC has properly started up, and is in a steady state condition when nSRESET goes high. The best place to probe for this is AFTER the ROUT pin, and before the 180k resistor using the lowest possible FET probe capacitance.

5. When nSRESET goes high, the RTC clock is accepted by the ARM via the internal mux, and the external configuration resistors are sensed for pull up or pull down resistors, and the configuration register is loaded accordingly. This sensing occurs on the JTAG lines, JTDI and JTCK, and certain Data lines.
6. These configuration straps tell the processor to operate from the GRF3w RF chip, or alternate chip, and that a certain clock frequency is provided at a certain port.
7. For this application, the 32kHz clock to the ARM is sensed and used, and is initially divided by 4, but after a few instructions, is instructed to divide by 1 internally.
8. The ARM programming RF programming sequence commands are then sent to program the 3w chip using the SPI interface. KEY: Verify that the SPI enable goes low (nSS[0]/GPIO[3]), and that the SPI clock and SPI Data signals are present (SK/GPIO[7] & SO/GPIO[6]) at CMOS levels to program the 3w. It is very important that the programming signals be free of any noise.
9. A wait of several ms occurs, and the LO + fractional-N PLL inside of the 3w starts up, and is divided down to provide an ACQCLK CMOS signal of **16.369MHz**.

   **NOTE 1**: Please verify this specific frequency if startup problems exist. There could be a problem with initial programming.
   If no output signal exists at ACQCLK or SIGN, there could be a problem with the GRF3w chip itself. Since this is a SiGe part, extreme care must be exercised in the assembly process to avoid ESD damage. Failure to exercise proper handling could damage this part. In addition, please verify that ALL voltages pins to the GRF3w device are energized, and at the proper voltage.

10. The ACQCLK signal is provided to the BB PLL multiplier, and the code multiplies the ACQCLK X3 for ARM clock operation. This is an internal switchover that occurs based on an available clock handoff.
11. The ACQCLK is also provided as a source to the UARTs, and a UARTdivider is programmed to provide a default baud rate of 57.6kbaud.
12. FOR GSW3 CODE: The BB TXA line sends a signal instruction the external processor to notify that all is operational.
13. FOR SLC3 CODE: There is no signaling between the GPS and the CP that the GPS will wait for. For SiRFLoc, after boot up and initialization the SLC will request the HW Configuration from the CP but there is no waiting. If the CP never answers the SLC will immediately start an autonomous fix.

    **NOTE 2**: If this signal is odd, or not present, the customer may have swapped the TX lines with RX lines. It is very, very important that the customer connect the external processors transmit pins, to our receive pins! (Many customers have missed this issue). Use of a null modem box may be of benefit in troubleshooting. Use of series resistors during layout will help to correct the problem, should it occur.

    If odd behavior is still present, it is highly recommended that the customer capture the waveforms in question, document the settings and test conditions, and provide to the appropriate SiRF FAE for further analysis. Recommended waveforms to capture are (a) nRESET, (b) RTCCLK, (c) SSN0, (d) ACQCLK, and POWER.

**It is also very important to capture**

**(a) SPI Enable,**

**(b) SPI clock, and**

**(c) SPI data transfer after nSRESET transitions high;**

To verify the correct programming is occurring. This occurs in a very narrow time period.
In addition, if replacing the RF chip, or BB chip does not solve the problem, and SiRF support is required, then we ask the customer to provide small (34 to 40 AWG) access wires to the 4 JTAG lines, along with nSRESET, and bring out to a stable off board test point for further troubleshooting at SiRF headquarters. These external wires should be less than 15cm in length, and should be PROPERLY anchored to a stable, off site board to avoid straining of the test pad solder joint, and damage to the tiny test pads! Most customers typically use perforated board material for a support platform. This may require securely mounting the board PERPENDICULAR to another test board, and then bringing the delicate leads to the new board with marked and defined probing points.
Do not send any hardware to SiRF until approved by Field Apps Engineering, and the proper schematics, parts layouts, and interface HW has been supplied.

**NOTE 3:** Please make sure that the parts are properly baked out at 85C for a minimum of 12 hours (24 preferred) prior to any replacement and removal attempt.

……..

**Section II: GSP3f +GRF3w STARTUP AND PROGRAMMING SEQUENCES**

**FOR INTERNAL BOOT MODE (WHEN FLASHING WITH SiRFlash )**

For those users who are having startup or flashing problems, please follow the suggested steps below to verify where any potential startup problems could be present.

In general, any problem should always be checked against a known good EVK unit. This is the best way to compare waveforms and signal levels that should be present at certain times.

If an EVK is not available, the following sequence of events should be reviewed and verified for proper behavior.

1. At initial power up, power supplies are switched on, power is supplied to input of the regulators and begins to stabilize, and oscillators start up and begin to stabilize. Verify these waveforms. It is assumed that the user has pulled D0 high with a switch prior to power up. This will trigger the internal boot ROM.
2. The Power On Reset (POR) generator senses this ramping voltage, and holds nSRESET low for a ***minimum*** of 200 (TBD)ms while voltages & waveforms stabilize.
3. The ARM processor in the BB requires a minimum of 40 stable clock cycles before operation can properly begin.
4. For the 3f+3w combination, most applications require the RTC clock to be present ***and stable with adequate amplitude*** (>900mVpp)to initiate the ARM operation. Therefore, the customer should verify that the RTC has properly started up, and is in a steady state condition when nSRESET goes high. The best place to probe for this is AFTER the ROUT pin, and before the 180k resistor using the lowest possible FET probe capacitance..

5. When nSRESET goes high, the RTC clock is accepted by the ARM via the internal mux, the internal BOOT ROM sequence is triggered, and the external configuration resistors are sensed for pull up or pull down resistors, and the configuration register is loaded accordingly. This sensing occurs on the JTAG lines, JTDI and JTCK, and certain Data lines.
6. These configuration straps tell the processor to operate from the GRF3w RF chip, or alternate chip, and that a certain clock frequency is provided at a certain port.
7. For this application, the 32kHz clock to the ARM is sensed and used, and is initially divided by 4, but after a few instructions, is instructed to divide by 1 internally.
8. The ARM programming commands are then sent to program the 3w chip using the SPI interface. KEY: Verify that the SPI enable goes low (nSS[0]/GPIO[3]), and that the SPI clock and SPI Data signals are present (SK/GPIO[7] & SO/GPIO[6]) at CMOS levels to program the 3w. It is very important that the programming signals be free of any noise.
9. A wait of several ms occurs, and the LO + fractional-N PLL inside of the 3w starts up, and is divided down to provide an ACQCLK CMOS signal of approximately 16.588MHz.

   **NOTE 1**: Please verify this specific frequency (+-2%) if startup problems exist. If not, there could be a problem with initial programming.
   If no output signals exist at ACQCLK or SIGN, there could be a problem with the GRF3w chip itself. Since this is a SiGe part, extreme care must be exercised in the assembly process to avoid ESD damage. Failure to exercise proper handling could damage this part. In addition, please verify that ALL voltages pins to the GRF3w device are energized, and at the proper voltage.

10. The ACQCLK signal is provided to the BB chip, and the code selects the ACQCLK for ARM clock operation. This is an internal switchover that occurs.
11. The ACQCLK is also provided as a source to the UARTs, and a divider is programmed to provide a default baud rate of 38.4kbaud .
12. The BB RXA line waits for a signal instruction (to) the BB processor to perform the next function.
13. Flashing occurs and can be monitored wit SiRFlash.

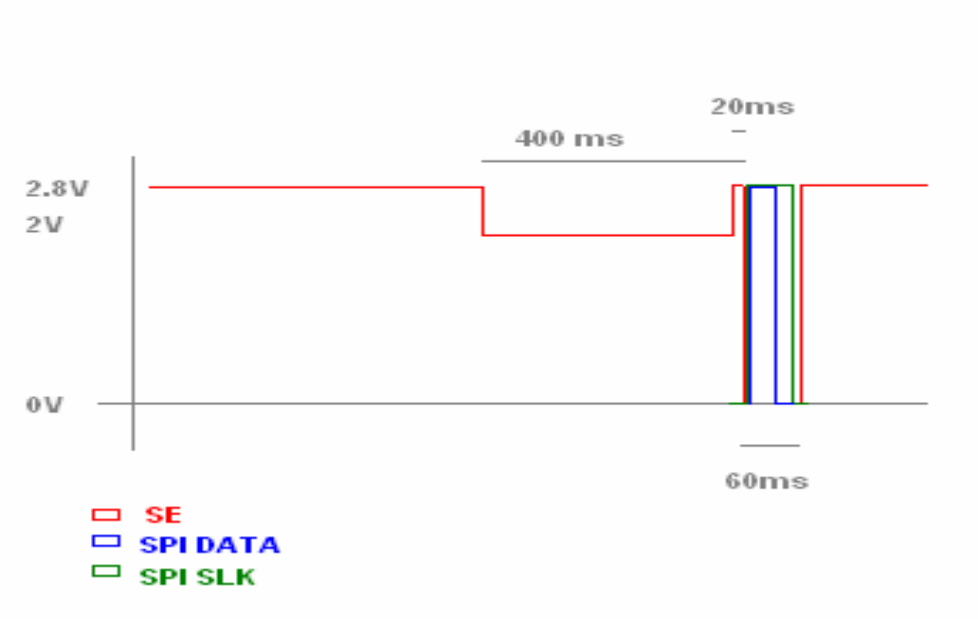
    **NOTE 2:** If the receiver is being flashed with SiRFlash, then a brief 4kbyte message (about 1 second) will appear on the GSP3f RECEIVE port (RXA) at CMOS levels. Silence on address and data lines will occur just before SiRFlash is executed.
    If this signal is odd, or not present, the customer may have swapped the TX lines with RX lines. It is very, very important that the customer connect the external processors transmit pins, to our receive pins! (Many customers have missed this issue). Use of a null modem box may be of benefit in troubleshooting.

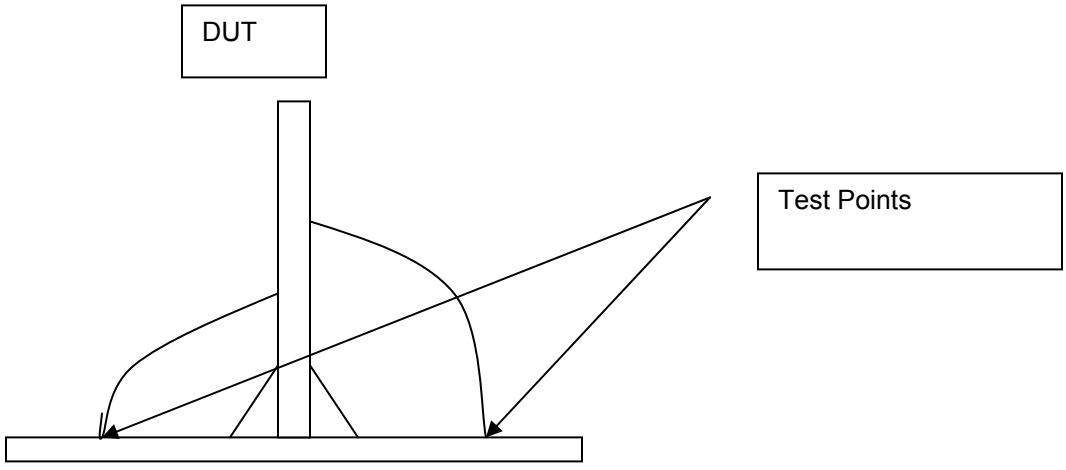
    If odd behavior is still present, it is highly recommended that the customer capture the waveforms in question, document the settings and test conditions, and provide to the appropriate SiRF FAE for further analysis.
    In addition, if replacing the RF chip, or BB chip does not solve the problem, then we ask the customer to provide small (34 to 40 AWG) access wires to the 4 JTAG lines, along with nSRESET, and bring out to a stable off board test point for further troubleshooting at SiRF headquarters. These external wires should be less than 15cm in length, and should be PROPERLY anchored to a stable, off site board to avoid straining of the test pad solder joint, and damage to the tiny test pads! This may require securely mounting the board

PERPENDICULAR to another test board, and then bringing the delicate leads to the new board with marked and defined probing points.

Do not send any hardware to SiRF until approved by Field Apps Engineering, and the proper schematics, parts layouts, and interface HW have been supplied

**NOTE 3**: Please make sure that the parts are properly baked out at 85C for a minimum of 12 hours (24 preferred) prior to any removal attempt.



## 12.6. Appendix C: Pin Definition Table & Summary

| **APPENDIX C: SiRFStar 3f Pin Definitions** | | | | | | | | | | | | | JC/01//05/05 SS3PINTABLE1_0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pin#** 100 BGA | | **NAME** (Primary intended operation) | Default Function @ reset ↑ | Alternate Function | Secondary Alt Function | Input/ Output | Default Output @ nSRESET ↑ | Default Input @ nSRESET ↑ | Internal **P/U** 100k nom | Internal P/D 100k nom | 1.5V I/O | 3.3v To I I/O | 3.3V5.2V I/O | **Notes** |
| | | AGCPWM (see GPIO2) | | | | I / O | | | | | | | | |
| **A7** | | CLKACQ | CLKACQ | | | IN | | | | | | X | | |
| | | nCTS (see nCS1) | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| **F8** | | nCS[0]/Reverse | nCS[0] | | | O | X | | X | | | | | Drives nCS_F & nADC_CS (Use of Ext RAMorROM w/opullup reqs review) |
| | | nCS[1]/GPIO[13]/nCTS (see GPIO13) | | | | | | | | | | X | | |
| | | nCS[2]/GPIO[14]/nRTS (see GPIO14) | | | | | | | X | | | X | | |
| | | nCS[3]/GPIO[15]/YCLK/Timersync (see GPIO15) | | | | | | | X | | | X | | |
| **E6** | | nCS_F | nCS_F | | | IN_F | | | X | | | ?? | | To Flash chip only |
| **K10** | | **GPIO[0]/** Reverse | GPIO[0] | Reverse | | I / O | | GPIO Input | | X | | X | | Alt=Reverse |
| **K9** | | **GPIO[1]**/ODO | GPIO[1] | ODO | | I / O | | GPIO Input | | X | | X | | Alt=Odometer |
| **A10** | | AGCPWM/**GPIO[2]** | GPIO[2] | AGCPWM | | I / O | | GPIO Input | | X | | X | | |
| **H5** | | nSS[0]/**GPIO[3]** | GPIO[3} | nSS[0] | | I / O | | GPIO Input | X | | | X | | |
| **A6** | | nSS[1]/**GPIO[4]**/MAG | GPIO[4] | nSS[1] | MAG | I / O | | GPIO Input | | | | X | | |
| **H5** | | SI/**GPIO[5]** | GPIO[5] | SI | | I / O | | GPIO Input | | X | | X | | Alt= ADC_DATA |
| **J6** | | SO/**GPIO[6]** | GPIO[6] | SO | | I / O | | GPIO Input | | X | | X | | |
| **J7** | | SK/**GPIO[7]** | GPIO[7] | SK | | I / O | | GPIO Input | | X | | X | | Alt= nADC_CLK |
| | | **GPIO[8]** (see RFPWRUP) | | | | | | OPUTPUT | | | | | | The only GPIO default exception at power up |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **K7** | | TIMEMARK/**GPIO[9]** | GPIO[9] | TIMEMARK | | I / O | | GPIO Input | | X | | X | | 1pps output |
| **J9** | | nEIT[0]/**GPIO[10]** | GPIO[10] | nEIT[0] | | I / O | | X | | | | X | | Ext Interrupt: Level sensitive input |
| | | N/A | | | | | | | | | | | | |
| | | N/A | | | | | | | | | | | | |
| | | N/A | | | | | | | | | | | | |
| **G10** | | nCS[1]/**GPIO[13]**/nCTS | GPIO[13] | nCS[1] | nCTS | I / O | | GPIO Input | | | | X | | Clear to send, only. No pullup present |
| **G9** | | nCS[2]/**GPIO[14]**/nRTS | GPIO[14] | nCS[2] | nRTS | I / O | | GPIO Input | X | | | X | | |
| **G8** | | nCS[3]/**GPIO[15]**/YCLK/Timersync | GPIO[15] | nCS[3] | YCLK/TSYNC | I / O | | GPIO Input | X | | | X | | Timexfer input, ↑trig, 100ns min, 1ms max<br>Must be set up for input mode |
| **J4** | | EA[0] | EA[0] | | | O | X | | | | | | | |
| **J3** | | EA[1] | EA[1] | | | O | X | | | | | | | |
| **K3** | | EA[2] | EA[2] | | | O | X | | | | | | | |
| **J2** | | EA[3] | EA[3] | | | O | X | | | | | | | |
| **J1** | | EA[4] | EA[4] | | | O | X | | | | | | | |
| **K2** | | EA[5] | EA[5] | | | O | X | | | | | | | |
| **K1** | | EA[6] | EA[6] | | | O | X | | | | | | | |
| **H2** | | EA[7] | EA[7] | | | O | X | | | | | | | |
| **H1** | | EA[8] | EA[8] | | | O | X | | | | | | | |
| **G1** | | EA[9] | EA[9] | | | O | X | | | | | | | |
| **F3** | | EA[10] | EA[10] | | | O | X | | | | | | | |
| **F2** | | EA[11] | EA[11] | | | O | X | | | | | | | |
| **F1** | | EA[12] | EA[12] | | | O | X | | | | | | | |
| **E3** | | EA[13] | EA[13] | | | O | X | | | | | | | |
| **E2** | | EA[14] | EA[14] | | | O | X | | | | | | | |
| **E1** | | EA[15] | EA[15] | | | O | X | | | | | | | |
| **C1** | | EA[16] | EA[16] | | | O | X | | | | | | | |
| **B1** | | EA[17] | EA[17] | | | O | X | | | | | | | |
| **G3** | | EA[18] | EA[18] | | | O | X | | | | | | | |
| **G2** | | EA[19] | EA[19] | | | O | X | | | | | | | |

| Pin# 100 BGA | | NAME (Primary intended operation) | Default Function | Alternate Function | Secondary Alt Function | Input / Output | Default Output @ nSRESET ↑ | Default Input @ nSRESET ↑ | Internal P/U 100k nom | Internal P/D 100k nom | | 3.3v Tol I/O | TBD | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | |
| **F10** | | ED[0] (Boot select) | ED[0]** | | | I / O | | X | | | | X | | At nSRESET ↑, if 1=Int. Boot (Flash load); 0=Ext Boot |
| **E10** | | ED[1] | ED[1]** | | | I / O | | X | | | | X | | 0=3w, 1=SC3RF |
| **D8** | | ED[2] | ED[2]** | | | I / O | | X | | | | X | | 0=boot frm ECLK, 1=boot frm RTCCLKorCLKACQ |
| **D10** | | ED[3] | ED[3]** | | | I / O | | X | | | | X | | 0=boot frm RTCCLK, 1=boot frm ECLKorCLKACQ |
| **C9** | | ED[4] | ED[4]** | | | I / O | | X | X | | | X | | |
| **C7** | | ED[5] | ED[5]** | | | I / O | | X | X | | | X | | |
| **C5** | | ED[6] | ED[6]** | | | I / O | | X | X | | | X | | |
| **B8** | | ED[7] | ED[7]** | | | I / O | | X | | | | X | | Must be pulled LOW |
| **E8** | | ED[8] | ED[8]** | | | I / O | | X | X | | | X | | Little Endian capability ONLY |
| **E9** | | ED[9] | ED[9]** | | | I / O | | X | X | | | X | | Pull H or L for frequency configuration |
| **D9** | | ED[10] | ED[10]** | | | I / O | | X | X | | | X | | Pull H or L for frequency configuration |
| **C10** | | ED[11] | ED[11]** | | | I / O | | X | X | | | X | | Pull H or L for frequency configuration |
| **B10** | | ED[12] | ED[12]** | | | I / O | | X | X | | | X | | Pull H or L for frequency configuration |
| **C6** | | ED[13] | ED[13]** | | | I / O | | X | X | | | X | | Pull H or L for frequency configuration |
| **B9** | | ED[14] | ED[14]** | | | I / O | | X | X | | | X | | |
| **B7** | | ED[15] | ED[15]** | | | I / O | | X | X | | | X | | |
| | | | | | | | | | | | | | | |
| | | nEIT[0]/GPIO[10] (see /GPIO10) | | | | | | | | | | | | |
| **K4** | | ECLK | ECLK | | | IN | | | | X | | X | | External clock input and Freq transfer (50MHz max) |
| | | | | | | | | | | | | | | |
| **A9** | | JTCK* | JTCK* | | | IN | | | | | | X | | Pull UP or DOWN with 10k for Refclk select |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **B6** | | JTDI* | JTDI* | | | IN | | | | | | X | | Pull UP or DOWN with 10k for Refclk select |
| **A8** | | JTDO | JTDO | | | O | | | | | | | | Pull UP or DOWN with 10k for Refclk select |
| **B4** | | JTMS | JTMS | | | IN | | | | | | X | | Pull UP or DOWN with 10k for Refclk select |
| **B5** | | JTRST | nJTRST | | | IN | | | | | | X | | Is actually an active low for the ARM7 |
| | | | | | | | | | | | | | | |
| | | MAG (see /GPIO4) | | | | | | | | | | | | |
| **H9** | | nMWE | nMWE | | | O | High | Verifyw/ds??? | | | | | | |
| **F9** | | nMOE | nMOE | | | O | High | Verifyw/ ds | | | | | | |
| | | MUL[0] (NOT USED) | | | | | | | | | | | | |
| | | MUL[1] (NOT USED) | | | | | | | | | | | | |
| **A3** | | ON_OFF | ON_OF F | | | IN | | | | | | X | | R.E trig'rd: For GSW3=gnd (usually), For SLC3=10k |
| **D1** | | PLL_FILTER | PLL_FI LTER | | | Ana | | | | | | | | Sensitive edge triggered input. Each rising/falling edge advances state machine. |
| | | | | | | | | | | | | | | |
| **C2** | | RIN | RIN | | | IN | | | | | | | | |
| **B2** | | ROUT | ROUT | | | O | | | | | | | | |
| | | | | | | | | | | | | | | |
| **J8** | | RXA | RXA | | | IN | | | X | | | | | |
| **H6** | | TXA | TXA | | | O | | | | | | | | |
| **K6** | | RXB | RXB | | | IN | | | X | | | | | |
| **K5** | | TXB | TXB | | | O | | | | | | | | |
| **A1** | | TMODE | TMODE | | | | | | | | | | | |
| | | nRTS (see /GPIO14) | | | | | | | | | | | | |
| | | nCTS (see /GPIO13) | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| **H10** | | RFPWRUP/GPIO[8] | RFPWR UP | GPIO[8 ] | | O | High w/ t.s. Cntrl | | | | | | | The only GPIO default exception at power up |
| **B3** | | nRESET (also calledRSTB) | nRESE T | | | OD | | | | | | ? | | O.D., Follows sSRESET at init pwrup, and reconfigs RFchip after pwr is reapplied. |
| **A4** | | nSRESET | nSRES ET | | | | | | | | | | | SYSTEM RESET. TIE TO JTRST &FlashRST |
| | | nRTS (see nCS2) | | | | | | | | | | | | |
| **H4** | | SCLK | SCLK | | | O | | | | | X | | | (Source clk *PLL)/ x = CPU CLK |
| **A5** | | SIGN_MAG | SIGN | MAG | | IN | | | | | | X | | For 3w, this input=SIGN. For alternate RF chips, muxed data input occurs. |

| Pin# 100 BGA | NAME (Primary intended operation) | Default Function | Alternate Function | Secondary Alt Function | Input / Output | Default Output @ nSRESET ↑ | Default Input @ nSRESET ↑ | Internal P/U 100k nom | Internal P/D 100k nom | 3.3v TOL I/O | TBD | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | |
| | nSS[0]/GPIO[3] (see GPIO3) | | | | | | | | | | | |
| | nSS[1]/GPIO[4]/MAG (see GPIO4) | | | | | | | | | | | |
| | SI/GPIO[5] (see GPIO5) | | | | | | | | | | | |
| | SO/GPIO[6] (see GPIO6) | | | | | | | | | | | |
| | SK/GPIO[7] (see GPIO7) | | | | | | | | | | | |
| | | | | | | | | | | | | |
| **A1** | TMODE | TMODE | | | IN | | | | | | | Reserved for testmode. O=normal oper. |
| | TIMEMARK/GPIO[9] (see /GPIO9) | | | | | | | | | | | |
| | TIMERSYNC (see nCS3/GPIO15) | | | | | | | | | | | Use for Time aiding input |
| | | | | | | | | | | | | |
| **C3** | VDD1 | | | | | | | | | | | VDD I/O RING PWR |
| **F7** | VDD2 | | | | | | | | | | | VDD I/O RING PWR |
| **G4** | VDD3 | | | | | | | | | | | VDD I/O RING PWR |
| **G5** | VDD4 | | | | | | | | | | | VDD I/O RING PWR |
| **J10** | VDD5 | | | | | | | | | | | VDD I/O RING PWR |
| **D6** | VDD_FLASH | | | | | | | | | | | FLASH input power |
| **F4** | VDD_PLL | | | | | | | | | | | Input pin to internal PLL LDO. |
| **F6** | VDD_REG1 | | | | | | | | | | | 1.5V Core regulator input PinA |
| **G6** | VDD_REG2 | | | | | | | | | | | 1.5V Core regulator Input PinB |
| **D2** | VDDPLL_0 | | | | | | | | | | | |
| **D3** | VDDK1 | | | | | | | | | | | Core (Kore) regulator output.Shared power ring |
| **E7** | VDDK2 | | | | | | | | | | | Core regulator output.Shared power ring. Decoupling 2.2uF cap needed |
| **C4** | VDD_RTC | | | | | | | | | | | Must decouple with 2.2uF |
| | | | | | | | | | | | | |
| **A2** | nWAKEUP | nWAKEUP | | | OD | | | | | X | | Use with 75k pullup to unswitched supply MUST NOT EXCEED 3.6V |
| | | | | | | | | | | | | |
| | YCLK (see nCS3/GPIO15) | | | | | | | | | | | |
| | | | | | | | | | | | | |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **J5** | | RESV1 | | | | O | X | | | | | | | BYTE SELECT: NOT AVAILABLE |
| **H7** | | RESV2 | | | | O | X | | | | | | | BYTE SELECT: NOT AVAILABLE |
| | | | | | | | | | | | | | | |
| **C8** | | GND1 | | | | | | | | | | | | |
| **D5** | | GND2 | | | | | | | | | | | | |
| **D7** | | GND3 (COREGND2) | | | | | | | | | | | | |
| **E4** | | GND4 (PLLGND 2) | | | | | | | | | | | | |
| **E5** | | GND5 (PLLGND 1) | | | | | | | | | | | | |
| **F5** | | GND6 | | | | | | | | | | | | |
| **H3** | | GND7 | | | | | | | | | | | | |
| **H8** | | GND8 | | | | | | | | | | | | |
| **G7** | | GND9 | | | | | | | | | | | | |
| **D4** | | GND_FLASH | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |

* Used to define REF CLOCK boot up selection w/ ext resistors

** Used as configuration straps during system reset

Ana=Analog function. Bypass with 0.01uF.

**OD**= Open Drain.

Default internal flash chip is SST 39VF400A

| *BOOT PULLUPS:* | *ED3* | *ED2* | *ED1* | |
|---|---|---|---|---|
| Reserved | 0 | 0 | 0 | |
| **Boot Clk= RTC** | **0** | **1** | **0** | |
| Boot Clk= ECLK (possible development) | 1 | 0 | | 1 or 0 (SW dependent) |
| **Boot Clk= CLKACQ** | **1** | **1** | **1** | |