FIBOCOM
Beyond Innovation

GTS-4E GPS Module
Hardware Integration Manual

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Revision History

Version	Date	Remarks
V1.0.0	2011-01-24	Initial Release

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Beyond Innovation

Preface

Manual Scope

This Manual provides hardware design instructions and information on how to set up production and final product tests.

Target Audience

This manual is intended for hardware developers who communicate with the GTS-4E module.

How to use this Manual

This manual has a modular structure. It is not necessary to read it from the beginning to the end. To help in finding needed information, a brief section overview is provided below:

1. Hardware Description: This chapter introduces the basics of function and architecture of the GTS-4E module.
2. Design-In: This chapter provides the Design-In information necessary for a successful design.
3. Electrical Specifications: This chapter provides information about testing of OEM receivers in production.
4. Mechanical Specifications: The Appendix includes a Reference Design, guidelines on how to successfully migrate to GTS-4E designs, and useful information about the different antenna types available on the market and how to reduce interference in your GPS design.
5. Layout: This chapter provides some layout matters needing attention for external circuit of GTS-4E module.
6. ESD Protection Measures: This chapter provides some ESD matters needing attention when no ESD device in the GTS-4E module.
7. Referent Design: This chapter provides a Referent Design for hardware development.

1 Hardware Description

1.1 Functional Overview

The GTS-4E designed by FIBOCOM basing on the SIRF-IV is a new generation of GPS receiving module, and also in price competitive advantage. It's a new 48-channel ultra-high sensitive GPS receiving module. Based on new highly integrated SIRF-IV chips and meticulously integration key parts of FIBOCOM, casting a brand-new GTS - 4E products, in the same chip specifications, product has faster GPS signals ability to capture, lower power consumption, more strong anti-jamming performance and more wide working voltage range.

GTS - 4E module designed with industrial requirements, using stamps package, can adapt to wet high temperature, electromagnetic interference etc odiously working environment. It is widely used in monitoring, positioning, mapping, navigation, security applications such as the ideal platform.

1.2 Naming rule of Part Number

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Serials number: 000:Base use(No DGPS and AGPS) 001:With DGPS and AGPS Other reserved			Reserve	Reserve	0: NO EEPROM 1: EEPROM ON	0: NO ESD 1: ESD ON	0:UART 1:SPI

Table 1：Naming rule of Part Number

Part Number in common use：

	UART	SPI	ESD	EEPROM	AGPS	DGPS	Lowpower
GTS-4E-00	●						●
GTS-4E-01		●					●
GTS-4E-02	●		●				●
GTS-4E-03		●	●				●
GTS-4E-20	●				●	●	●
GTS-4E-21		●			●	●	●
GTS-4E-22	●		●		●	●	●
GTS-4E-23		●	●		●	●	●
GTS-4E-24	●			●	●	●	●
GTS-4E-26	●		●	●	●	●	●

Table 2：Part Number in common use

1.3 Block Diagram

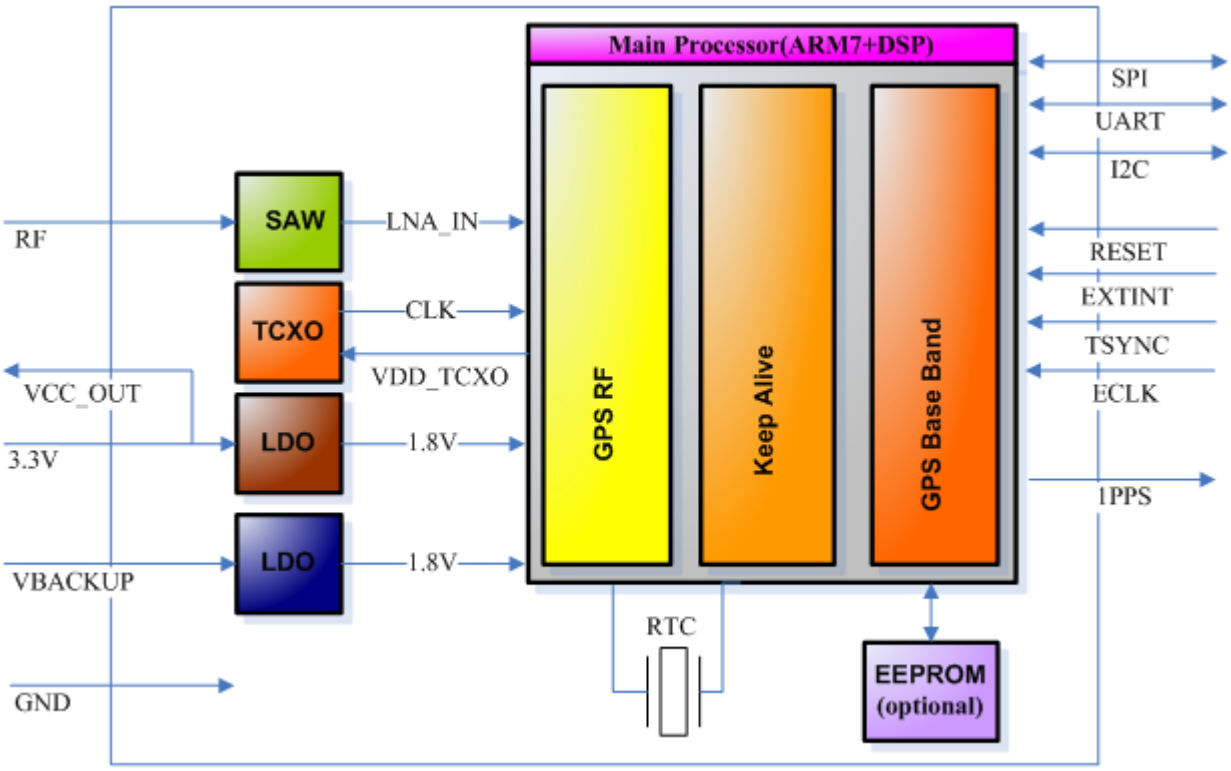


Figure 1: Hardware Block Schematic

2 Design-In

2.1 Power Management

2.1.1 Connecting Power

GTS-4E receivers have two power supply pins: VCC, V_BCKP.

2.1.1.1 VCC - Main Power

The main power supply is fed through the **VCC** pin. During operation, the current drawn by the GTS-4E GPS module. It is important that the system power supply circuitry is able to support the peak power (see datasheet for specification) for a short time. In order to define a battery capacity for specific applications the sustained power figure shall be used.

2.1.1.2 V_BACK - Backup Battery

The **V_BACK** should **always on both in Sleep mode and working on mode**. That is to say only **VCC - Main** Power can not power on the module, it needs both **VCC - Main** Power and **V_BACK**.There are three ways for you to connection **V_BACK** pin:

1. Backup Battery
2. Directly Connect to or by switcher to **VCC - Main** Power
3. GPIO

In case of a power failure on pin **VCC**, the real-time clock and backup RAM are supplied through pin **V_BACK**.This enables the GTS-4E receiver to recover from a **VCC - Main** power failure with either a Hotstart or a Warmstart(depending on the duration of **VCC** outage) and to maintain the configuration settings. If no backup battery is connected, the receiver performs a Coldstart at power up.

2.1.2 Power Modes

GTS-4E offer five power modes for user, list as:

- Full Power Mode: The module will enter Hibernate state after first power up with factory configuration settings. TheNavigation mode will start after waking up from Hibernate state in cold start mode by sending ON_OFF signal interrupt pulse from host. Power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as full on, Full Power or Navigation mode.Navigation is available and any configuration settings are valid s long as the VDD power supply is active. When the VDD is powered off, settings are reset to factory configuration and receiver performs a cold start on next power up.VDD supply is intended to be kept active all the time and navigation activity is suggested to be controlled to low quiescent Hibernate state via ON_OFF control input.

- Deep Sleep Mode:By cut **VCC - Main** Power off with **V_BACK** on.

- Advanced Power Management (APM): APM allows power savings while ensuring that the quality of the solution is maintained when signal levels drop. APM does not engage until all necessary information is received. Host can configure e.g. number of APM cycles(continuous or up to 255), time between fixes (10… 180 sec), Power duty cycle (5…100%) and max position error. Rest of the time the receiver stays in Hibernate state. This mode is configurable with SiRF binary protocol message ID53.

- Push-to-Fix Mode (PTF): In this mode the receiver is configured to wake up periodically, typically every 1800 sec (configurable range 10… 7200 sec), for position update and to collect new ephemeris data from rising satellites. Rest of the time the receiver stays in Hibernate state. When position update is needed, the host can wake up the receiver by ON_OFF control input interrupt (pulse low-high-low >90us after which the receiver performs either Snap or Hot start and a valid fix is available within 1… 8 seconds typ.This mode is configurable with SiRF binary protocol message

ID151 & 167.

- Adaptive TricklePower (ATP): In this mode the receiver stays at full on power state for 200… 900ms and provides a valid fix. Between fixes with 1… 10 sec interval the receiver stays in Hibernate state. ATP mode is configurable with SiRF binary protocol message ID151. The receiver stays once in while in Full on power mode automatically (typ.every 1800 sec) to receive new ephemeris data from rising satellites or if received signal levels drop below certain level.

2.2 Interfaces

There are two communication interfaces, Uart and SPI, for user port. It is valid for different part number(refer to **Table 1：Naming rule of Part Number**).

For uart port the default protocol for host communication is NMEA 4800 baud. Protocol is switchable to SiRF binary OSP (One Socket Protocol) by NMEA protocol command $PSRF100.

Default NMEA message configuration: $GPGGA, $GPGSA and $GPRMC rate every second (in this order) and $GPGSV messages (can be 1… 4) every 5 seconds (sent after $GPGSA message).

GTS-4E also offer a I2C bus for external EEPROM and Accelerometer, it is valid in some part number.

2.2.1 Host Port UART

UART is normally used for GPS data reports and receiver control. Serial data rates are selectable from 1200 baud to 1.8432 Mbaud. Default baud rate is 4800 baud; default protocol is NMEA(protocol and baud rate can be configured by NMEA $PSRF100 message). RX signal is suggested to be pulled up externally when not used.

2.2.2 Host Port SPI

The host interface SPI is a slave mode SPI:

- Supports both SPI and Microwire formats
- An interrupt is provided when the transmit FIFO and output serial register (SR) are both empty
- The transmitter and receiver each have independent 1024B FIFO buffers
- The transmitter and receiver have individual software-defined 2-byte idle patterns of 0xA7 0xB4
- Clock polarity: default SPI mode 1 (CPOL=0; CPHA=1) i.e. data is captured on the clock's falling edge and data is propagated on a rising edge
- SPI detects synchronization errors and is reset by software

- Supports a maximum clock of 6.8MHz.
- Signals: TX (SPI_DO, MISO), RX (SPI_DI, MOSI), CTS_N (SPI_CLK) and RTS_N (SPI_SS_N)

At system level the slave has no way of forcing data to the master to indicate it is ready for transmission; the master must poll the client periodically. Since the specified idle byte pattern for both receive and transmit is A7 B4, the master can transmit this idle pattern into the slave repeatedly.If the master receives idle patterns back from the slave, it indicates that the slave currently has nothing to transmit but is ready to communicate. Default protocol is NMEA (protocol can be configured by NMEA $PSRF100 message).

On the receive side, the host is expected to transmit idle pattern A7 B4 when it is querying the module's transmit buffer, unless it has traffic to send to the module. In this way, the volume of discarded bytes is kept nearly as low as in the UART implementation because the hardware does not place most idle pattern bytes in its RX FIFO.

The FIFO thresholds are placed to detect large messages requiring interrupt-driven servicing. On the transmit side, the intent is to fill the FIFO only when it is disabled and empty. In this condition, the SPI driver software loads as many queued messages as can completely fit in the FIFO. Then the FIFO is enabled. The host is required to poll messages until idle pattern bytes are detected. At this point the FIFO is empty and disabled, allowing the SPI driver to again respond to an empty FIFO interrupt and load the FIFO with any messages in queue.

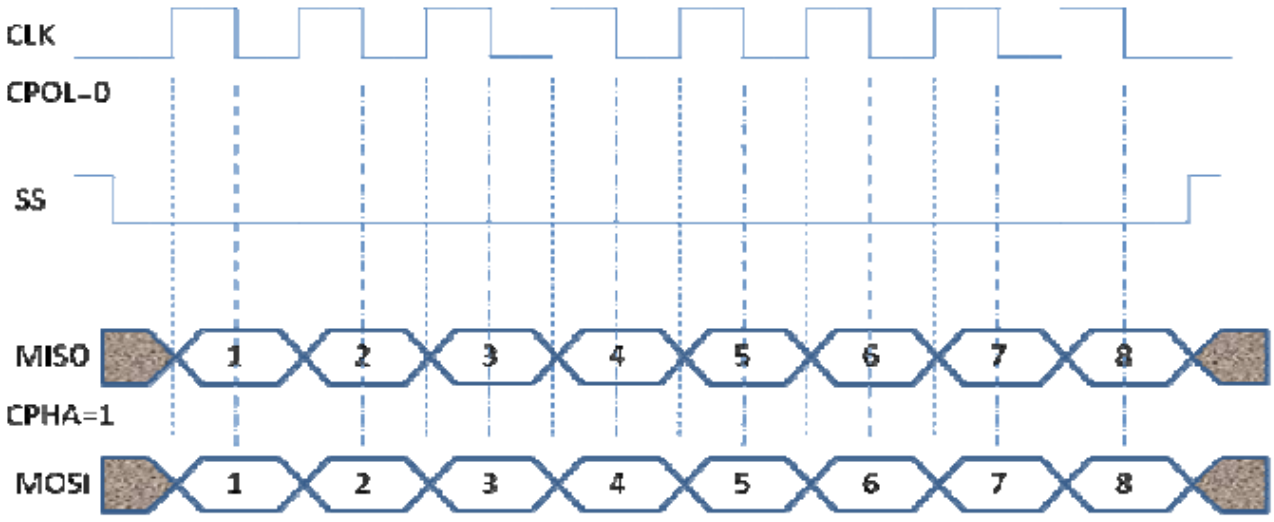


Figure 2: SPI host port timing diagram, SPI mode 1 (assuming one byte transfer)

2.2.3 Dead Reckoning I2C bus

The DR_I2C bus (master) provides optional connectivity to the following devices:

- Optional Dead Reckoning sensors (e.g. 3-D Accelerometer)
- Optional connectivity to EEPROM for Client Generated Extended Ephemeris (CGEE) data storage
- Optional ROM patch code storage to EEPROM and upload to IT430

.

The accelerometer MEMS sensor provides stationary detection, which allows to reduce the position spread when stationary with weak GPS signals e.g. indoors. Other features will follow like Point & Tell, i.e. attitude (heading) information based on 3-D compass (contact Fastrax support for details). When MEMS sensor is used connect also the sensor's INT output to IT430's EIT input. The bus signals require external pull up resistors 2.2kohm on both signals. Connect both signals to GND (or pull up) when not used.

DR I²C interface supports:

- Common sensor formats (Kionix, KXTF9-4100 device)
- Common EEPROM data formats (STMicroelectronics, M24M01, 1 Mbit device)
- Typical data lengths (command + in/data out) of several bytes
- Standard I²C bus maximum data rate 400kbps
- Minimum data rate 100kbps

2.2.4 ON_OFF control input

The ON_OFF control input must be used by the host to wakeup the module after first power up and to control the receiver activity between Normal and Hibernate states and also to generate interrupt in Push-to-Fix and SiRFAware modes of operation.

The module will boot to Hibernate state after power up. First ON_OFF interrupt wakes up the module for Normal (Navigation) operation. Consequent ON_OFF interrupts switch the operation mode between Hibernate and Navigation modes.

The ON_OFF interrupt is generated by rising edge of a low-high-low pulse, which should be longer than 90us and less than 1s (suggestion is abt. 100ms pulse length). Do not generate ON_OFF interrupts less than 1 sec intervals. Especially take care that any multiple switch bounce pulses are filtered out.

During Hibernate state the I/O Keep Alive is still active, thus I/O signals keep respective states except TX and RX signals, which are configured to high input impedance state.

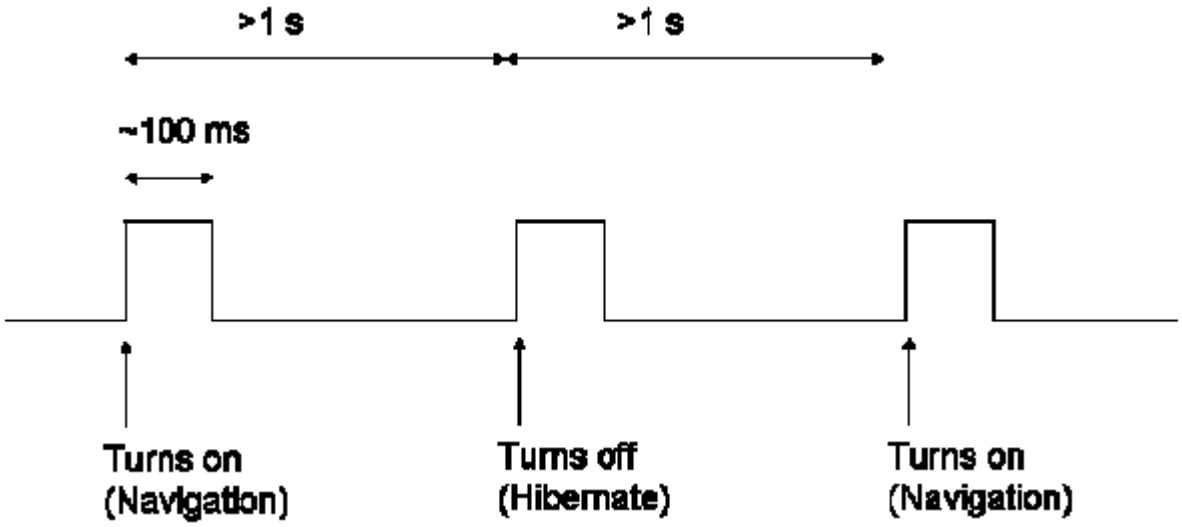


Figure 3: Suggested ON_OFF Hibernate control timing diagram.

2.2.5 Antenna input

The module supports passive and active antennas. The antenna input RF_IN impedance is 50 ohms and it provides also a bias supply low-pass filtered form VDD_ANT supply. The RF input signal path contains first a SAW band-pass filter, which provides good out-of-band protection against GPS blocking caused by possible near-by wireless transmitters.

Note that antenna input is ESD sensitive. With passive antennas the ESD performance can be improved by connecting VDD_ANT supply input to GND. Also an external TVS diode with low capacitance (<0.5pF, e.g. Infineon ESD0P2RF) can be used to improve RF-input ESD capability.

With passive antenna the suggested power mode is LDO (default) since Switcher mode will reduce sensitivity by about 4dB (typ.). Note that with an active antenna usage there is no effect of the power mode used and both LDO and Switcher mode give equal performance.

2.2.6 Active GPS antenna

The customer may use an external active GPS antenna when antenna cable loss exceeds > 1dB.It is suggested the active antenna has a net gain including cable loss in the range from +7 dB to +25 dB. Specified sensitivity is measured with external low noise (NF<1dB, G>15dB) amplifier, which gives about 2dB advantage in sensitivity when compared to a passive antenna.

An active antenna requires certain bias voltage, which can be supplied externally via VDD_ANT supply input. De-couple externally the VDD_ANT input; see the application circuit diagram in chapter 6. The external bias supply must provide limitation of the max current below 150mA during e.g. antenna signal short circuit condition.

When the module is in Hibernate state, the antenna bias can be switched off externally by using WAKEUP signal output to switch off VDD_ANT supply, see e.g. Application Circuit Diagram.

2.2.7 Time Mark TM

The TM output signal provides pulse-per-second (1PPS) output pulse signal for timing purposes.Pulse length (high state) is 200ms about 1us accuracy synchronized at rising edge to full UTC second.The firmware may support optionally other output functions from TM signal, like GPS_ON output for e.g. external LNA power control or RTC_CLK, which outputs buffered RTC clock signal at 32768 Hz; contact FIBOCOM support for details.

2.2.8 ECLK

The ECLK is reserved for external clock input with special variant for A-GPS frequency aiding.The input is suggested to be connected to GND when not used.

2.2.9 TSYNC

TSYNC input is reserved for external time aiding with a special variant used for A-GPS. The input is suggested to be connected to GND when not used.

2.3 HW Information

2.3.1 Pin Assignment

No.	Name	I/O	Description
1	RESERVE		Do not connect
2	SS_N	I	SPI Slave Select
3	TIMEPULSE	O	Time pulse (1PPS)
4	ON/OFF	I	External ON/OFF Signal
5	ECLK	I	ECLK clock input for frequency aiding applications
6	TSYNC	I	TSYNC is the time transfer strobe input used in AGPS precise time aiding. Edges on this pin latch ACQCLK counter values, this helps message data to transfer time information between

			systems.
7	RESERVE		Do not connect
8	RESERVE		Do not connect
9	VCC_RF	O	Output Voltage RF section
10	GND	I	Ground
11	RF_IN	I	GPS signal input
12	GND	I	Ground
13	GND	I	Ground
14	MOSI	I	SPI MOSI
15	MISO	O	SPI MISO
16	SCK	I	SPI Clock
17	RESERVE		Do not connect
18	SDA	I/O	DDC Data
19	SCL	I/O	DDC Clock
20	TxD	O	Serial Port 1
21	RxD	I	Serial Port 1
22	V_BACK	I	Backup voltage supply
23	VCC	I	Supply voltage
24	GND	I	Ground

Table 3: Pin Assignment

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply voltage (VCC)	Vcc	-0.5	5.5	V
Backup battery voltage (V_BCKP)	V_BACK	-0.5	5.5	V
Input pin voltage		-0.5	3.6	V
Storage temperature	Tstg	-40	85	°C

Table 4: Absolute Maximum Ratings

3.2 Operating Condition

Paramete	Symbol	Min	Typ	Max	Units
Power supply voltage (VCC)	Vcc	2.7	3.0	5.5	V
Sustained supply current					

Backup battery voltage	V_BACK	1.8	3.0	5.5	V
Backup battery current(Cut Main Power)	I_BACK	50	550	600	uA
Backup battery current(By ON/OFF)		50	130	150	
Input pin low voltage	Vil	-0.4	-	0.45	V
Input pin high voltage	Vih	1.26	-	3.6	V
Output pin low voltage for TXD	Voh	VCC-0.1	-	VCC	V
Output pin low voltage	Vol	-	-	0.40	V
Output pin high voltage	Voh	1.35	1.8	1.8	V
Antenna gain					
Receiver Chain Noise Figure	SEN	2.1	3.1	3.6	dB
AGC at minimum gain setting	-	-	-	62	dBm
AGC at mid gain setting	-	73.5	85.0	96.5	dB
Operating temperature	Topr	-40	-	85	°C

Table 5: Operating Condition

4 Mechanical Specifications

Parameter	**Specification**
A	16.0 +0.6/-0.1mm [628.8 +24/-4mil]
B	12.2 ±0.1mm [479.5 ±4mil]
C	2.4 ±0.2mm [94.3 ±8mil]
D	1.0 +0.3/-0.1mm [39.3 +18/-4mil]
E	1.1 ±0.1mm [43.2 ±4mil]
F	3.0 ±0.1mm [117.9 ±4mil]
G	1.1 ±0.1mm [43.2 ±4mil]
H	1 +0.3/-.01mm [39.3 +18/-4mil]]
Weight	1.6g

Table 6: Mechanicl Specifications

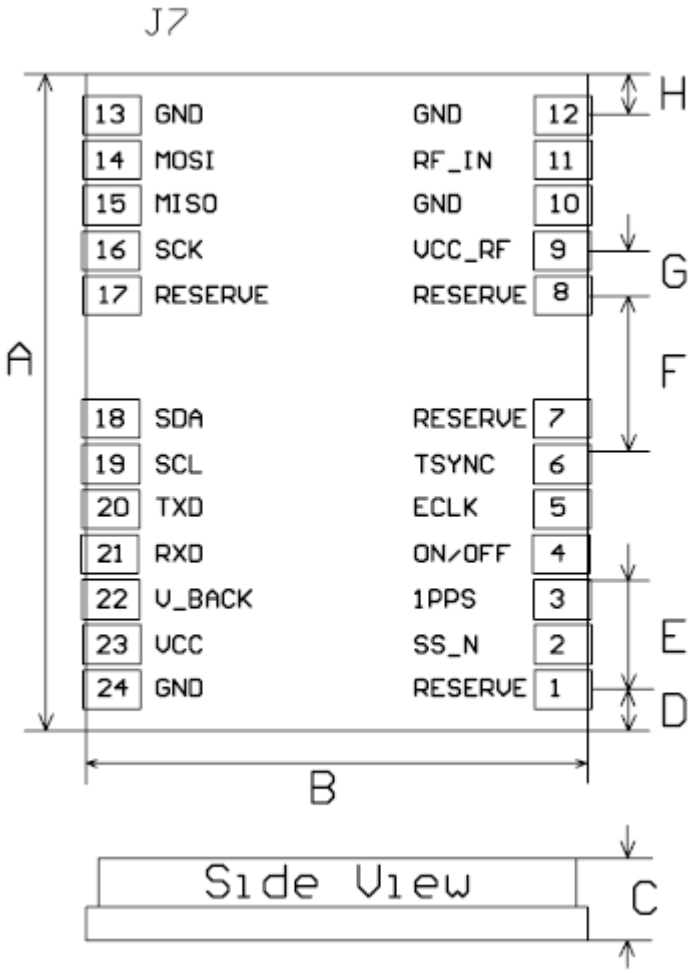


Figure 4: Mechanical Specifications

5 Layout

This section provides important information for designing a reliable and sensitive GPS system.GPS signals at the surface of the Earth are about 15dB below the thermal noise floor. Signal loss at the antennaand the RF connection must be minimized as much as possible. When defining a GPS receiver layout, the placement of the antenna with respect to the receiver, as well as grounding, shielding and jamming from other digital devices are crucial issues and need to be considered very carefully.

5.1 Paste Mask

Figure 5 shows the recommended positioning of the Paste Mask, the Copper and Solder masks. These are recommendations only and not specifications. Note that the Copper and Solder masks have the same size and position.

To improve the wetting of the half vias, reduce the amount of solder paste under the module and

increase the volume outside of the module by defining the dimensions of the paste mask to form a T-shape (or equivalent) extending beyond the Copper mask as shown in Figure 5. The solder paste should have a total thickness of 175 to 200 µm.

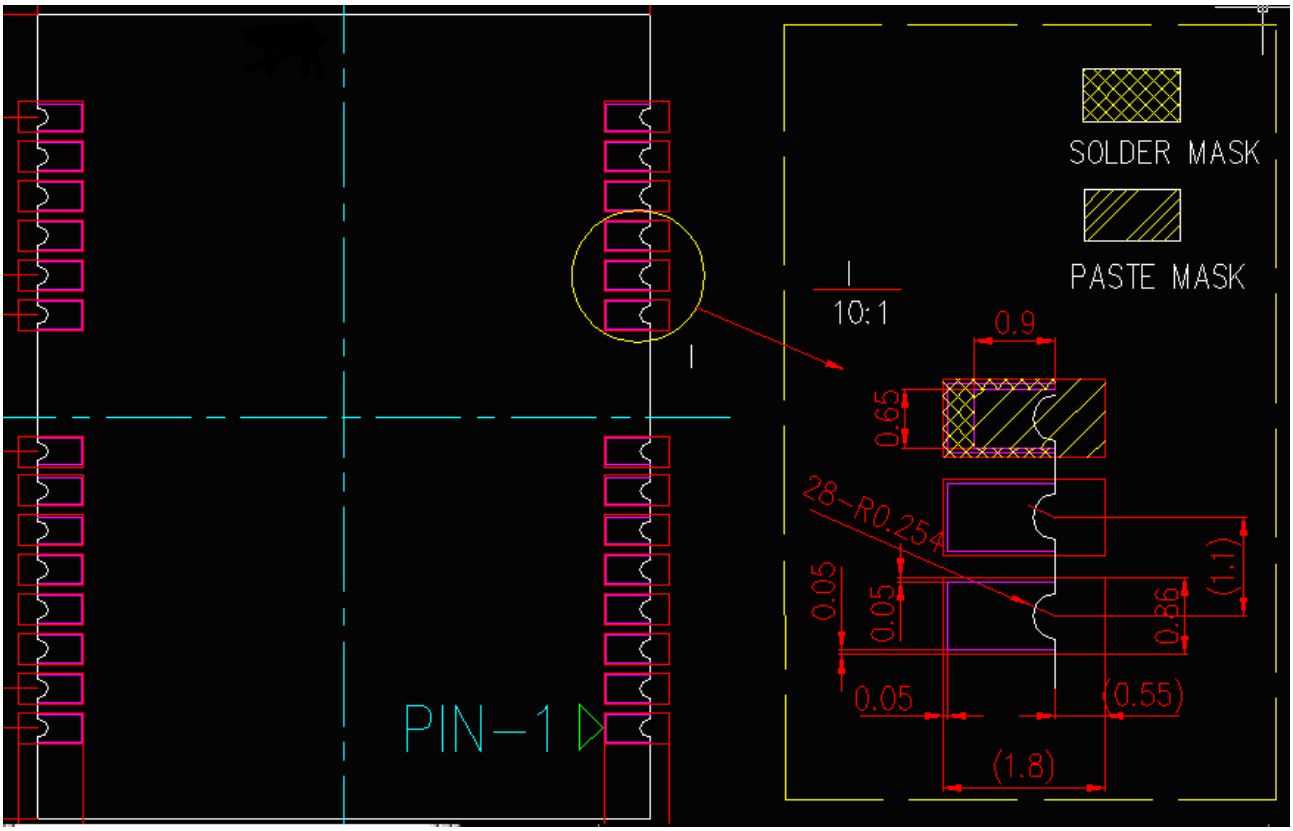


Figure 5： Recommendations for copper, solder and paste masks with enlargement

Note:

1. The paste mask outline needs to be considered when defining the minimal distance to the next component.

2. The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

5.2 Placement

A very important factor in achieving maximum GPS performance is the placement of the receiver on the PCB. The connection to the antenna must be as short as possible to avoid jamming into the very sensitive RF section.

Make sure that RF critical circuits are clearly separated from any other digital circuits on the system

board. To achieve this, position the receiver digital part towards your digital section of the system PCB. Care must also be exercised with placing the receiver in proximity to circuitry that can emit heat. The RF part of the receiver is very sensitive to temperature and sudden changes can have an adverse impact on performance.

Note:

The RF part of the receiver is a temperature sensitive component. Avoid high temperature drift and air vents near the receiver.

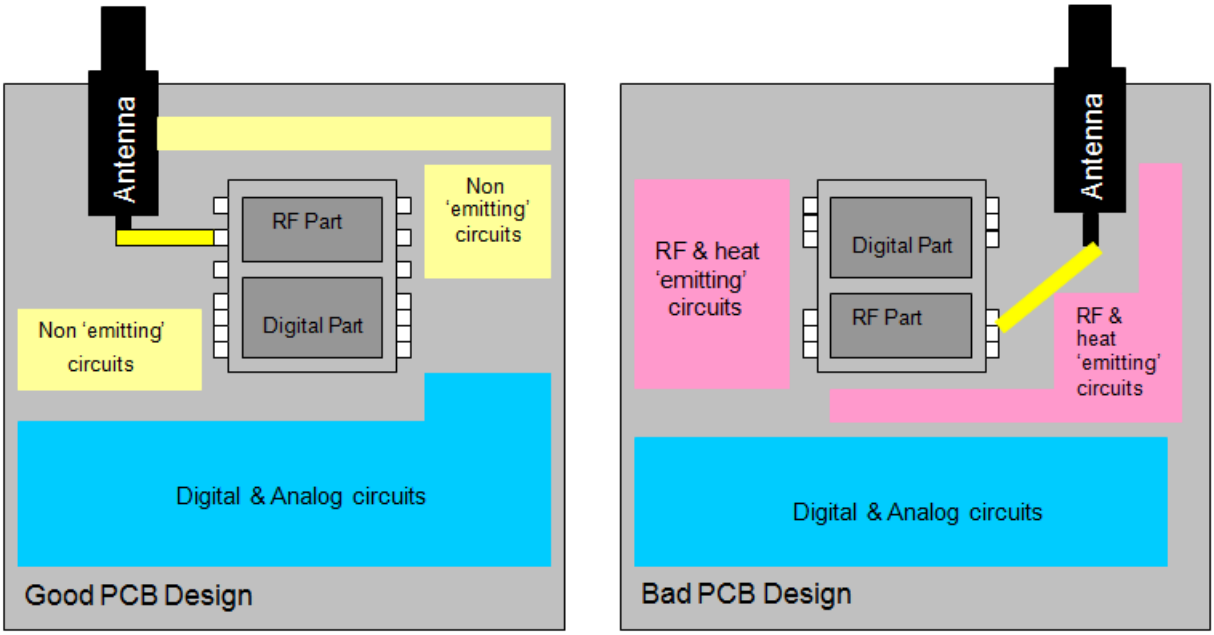


Figure 6： Antanna Placement

5.3 Antenna Connection and Grounding Plane Design

GTS-4E module can be connected to passive patch or active antennas. The RF connection is on the PCB and connects the RF_IN pin with the antenna feed point or the signal pin of the connector, respectively. The Figure below illustrates connection to a typical five-pin RF connector. Depending on the actual size of the ground area, additional vias should be placed in the outer region. In particular, the edges of the ground area should be terminated with a dense line of vias.

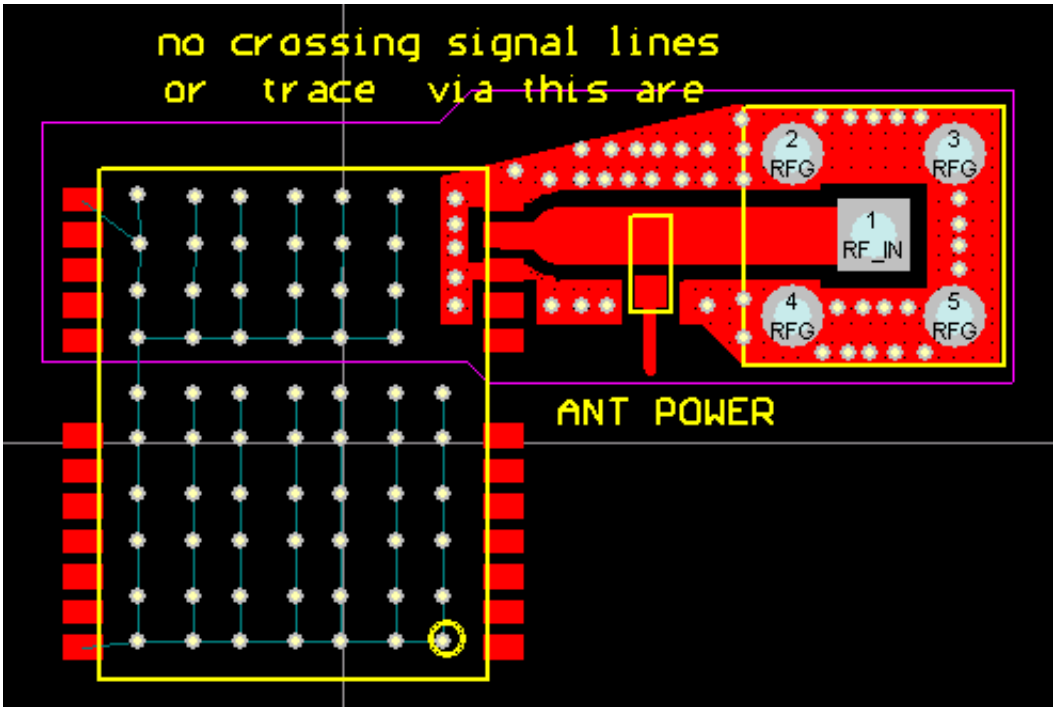


Figure 7： Recommanded Layout Design

As seen in Figure 7, an isolated ground area is created around and below the RF connection. This part of the circuit MUST be kept as far from potential noise sources as possible. Make certain that no signal lines cross, and that no signal trace vias appear at the PCB surface within the area of the red rectangle. The ground plane should also be free of digital supply return currents in this area. On a multi layer board, the whole layer stack below the RF connection should be kept free of digital lines. This is because even solid ground planes provide only limited isolation.

The impedance of the antenna connection has to match the 50 Ohm impedance edof the receiver. To achieve an impedance of 50 Ohms, the width W of the micro strip has to be chosen depending on the dielectric thickness H, the dielectric constant ε_r of the dielectric material of the PCB and on the build-up of the PCB.To make good impedance

General design recommendations:

The length of the micro strip line should be kept as short as possible. Lengths over 2.5 cm (1 inch) should be avoided on standard PCB material and without additional shielding.

Distance between micro strip line and ground area on the top layer should at least be as large as the dielectric thickness.

Routing the RF connection close to digital sections of the design should be avoided.

To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

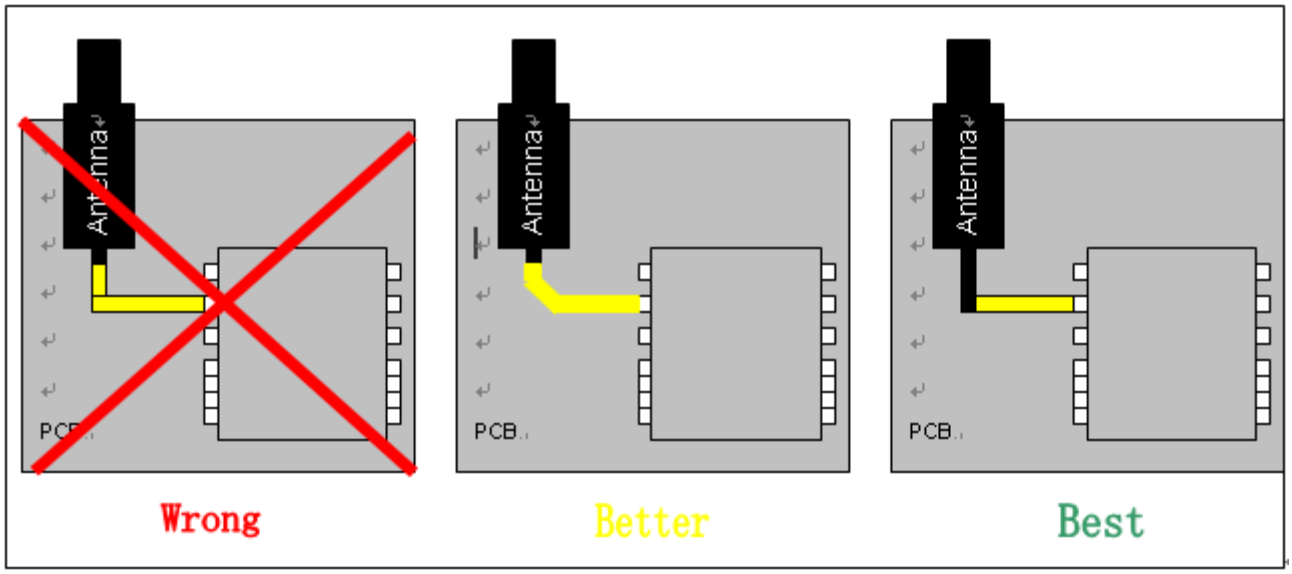


Figure 8： RF Line Recommanded Design

- Routing of the RF-connection underneath the receiver should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small (some 100 µm) and has huge tolerances (up to 100%). Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.
- In order to avoid reliability hazards, the area on the PCB under the receiver should be entirely covered with solder mask. Vias should not be open.

5.4 Antenna and Antenna Supervisor

GTS-4E module receive L1 band signals from GPS satellites at a nominal frequency of 1575.42 MHz. The RF signal is connected to the **RF_IN** pin.

GTS-4E module can be connected to passive or active antennas.

Note:

For GTS-4E receivers, the total preamplifier gain (minus cable and interconnect losses) must not exceed 50 dB. Total noise figure should be below 3 dB.

5.4.1 Passive Antenna

A design using a passive antenna requires more attention regarding the layout of the RF section.

Typically a passive antenna is located near electronic components; therefore care should be taken to reduce electrical 'noise' that may interfere with the antenna performance. Passive antennas do not require a DC bias voltage and can be directly connected to the RF input pin RF_IN. Sometimes, they may also need a passive matching network to match the impedance to 50 Ohms.

Note:

- Some passive antenna designs present a DC short to the RF input, when connected. If a system is designed with antenna bias supply AND there is a chance of a passive antenna being connected to the design, consider a short circuit protection.
- All GTS-4E receivers have a built-in LNA required for passive antennas.

5.4.2 Active Antenna

Active antennas have an integrated low-noise amplifier. They can be directly connected to **RF_IN**. If an active antenna is connected to **RF_IN**, the integrated low-noise amplifier of the antenna needs to be supplied with the correct voltage through an external inductor. Usually, the supply voltage is fed to the antenna through the coaxial RF cable. Active antennas require a power supply that will contribute to the total GPS system power consumption budget with additional 5 to 20 mA typically. Inside the antenna, the DC component on the inner conductor will be separated from the RF signal and routed to the supply pin of the LNA.

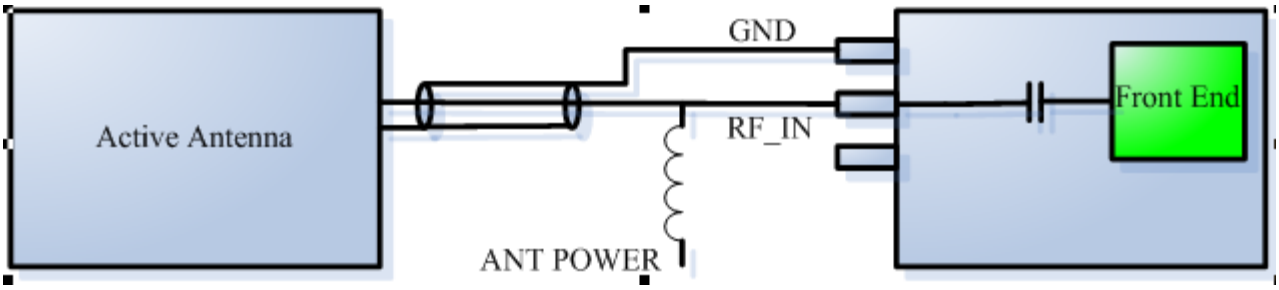


Figure 9：Active antenna biasing

Generally an active antenna is easier to integrate into a system design, as it is less sensitive to jamming compared to a passive antenna. But an active antenna must also be placed far from any noise sources to have good performance.

Note:

- Antennas should only be connected to the receiver when the receiver is not powered. Do not connect or disconnect the Antenna when the GTS-4E receiver is running as the receiver calibrates the noise floor on power-up. Connecting the antenna after power-up can result in prolonged acquisition time.
- Supply voltage Should connect to RF_IN by inductor.
- To test GPS signal reacquisition, it is recommended to physically block the signal to the antenna, rather than disconnecting and reconnecting the receiver.

For optimal performance, it is important to place the inductor as close to the microstrip as possible. Figure 10 illustrates the recommended layout and how it should not be done.

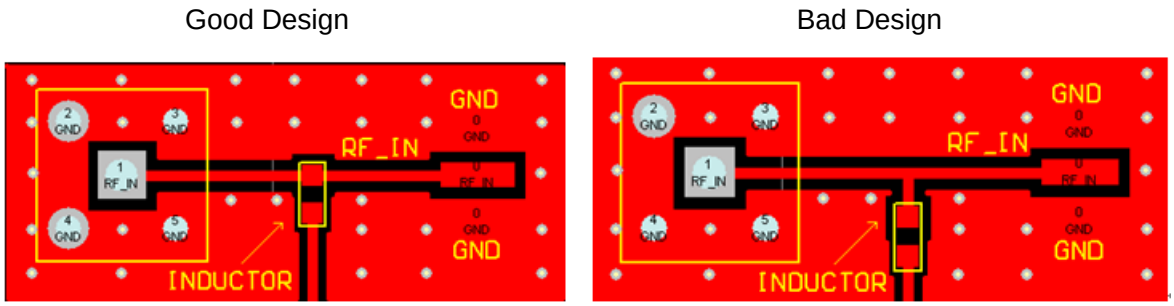


Figure 10：Recommended layout for connecting the antenna bias voltage

6 ESD Protection Measures

6.1 ESD Precautions for Antennas

Antennas are an area of particular ESD sensitivity for GPS receivers. For improved resistance to external transient voltage spikes ESD protection circuits can be used. For passive antennas introduce a coil between the module and the patch (see Figure 11). By using a low capacitance ESD protection diode in an active antenna design it is possible to achieve ESD protection IEC-61000-2-4 Level 1.

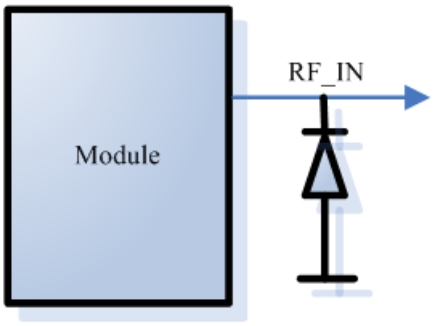
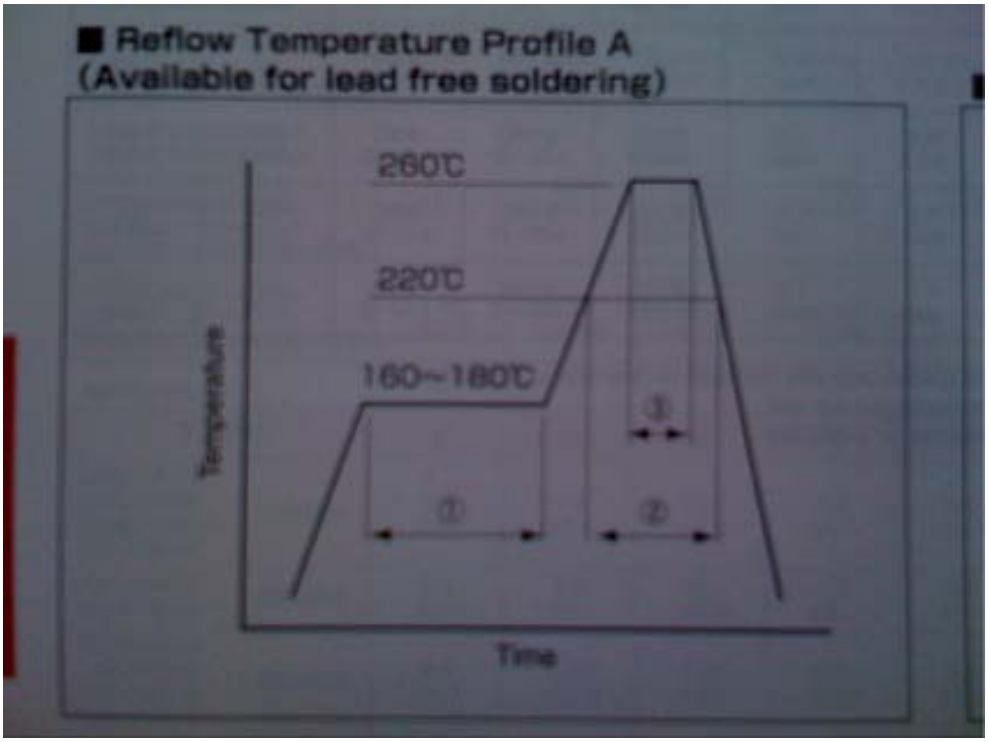


Figure 11：ESD Recommended Design

7 Reflow Refference



①	Preheat	160～180℃	120sec.
②	Primary Heat	220℃	120sec.
③	Peak	260℃	10sec. max.