Architecture Highlights

Compatible with Multiple SiRF Products

- Compatible with SiRFstarII IP, SiRFstarIII IP, and SiRFsoft
- Compatible with SiRFatlas, SiRFtitan, and SiRFprima SoCs

0.18 µm SiGE BiCMOS RF Process Technology

- Low power RF core voltage for reduced power consumption
- Extensive use of new digital design libraries and improved design for testability (DFT)

Enhanced RF Performance

- Outstanding linearity and gain stability over temperature
- Internally matched 50 Ω RF input
- Improved noise figure

Improved Jamming Immunity

- Selectable Wide/Narrow IF filter bandwidths
- Improved 1 dB compression

Easy Integration

- On-chip regulator reduces part count
- No RF matching components required

Product Highlights

Designed for Flexibility and High Levels of Integration

- SiRF Baseband Engine Mode: 2-bit sampling at 16 f_0
- SiRFsoft Engine Mode: 1- or 2-bit sampling at a 4, 8, or 16 f_0
- SiRF SoC Mode (SiRFatlas, SiRFtitan, and SiRFprima): 2-bit sampling at 16 f_0
- Integrated dual bandwidth IF filter
- Integrated VCO and Loop Filter
- Integrated LDO
- Integrated RTC oscillator and monitor
- Separate main and I/O power supply pins
- Supports a wide range of external references between 13 MHz and 38.4 MHz using Frac-N
- 14 mA current consumption with 11 mA low current mode
- 1.8 V core operating voltage
- IF test point access
- 4-wire SPI interface for programming of registers
- High speed CMOS interface to baseband
- 2-bit SIGN/MAG multiplexed onto a single pin or onto separate pins
- Single-stage down conversion
- Small 4 mm x 4 mm 24-pin QFN package
- Requires minimum external components
- On-chip AGC option

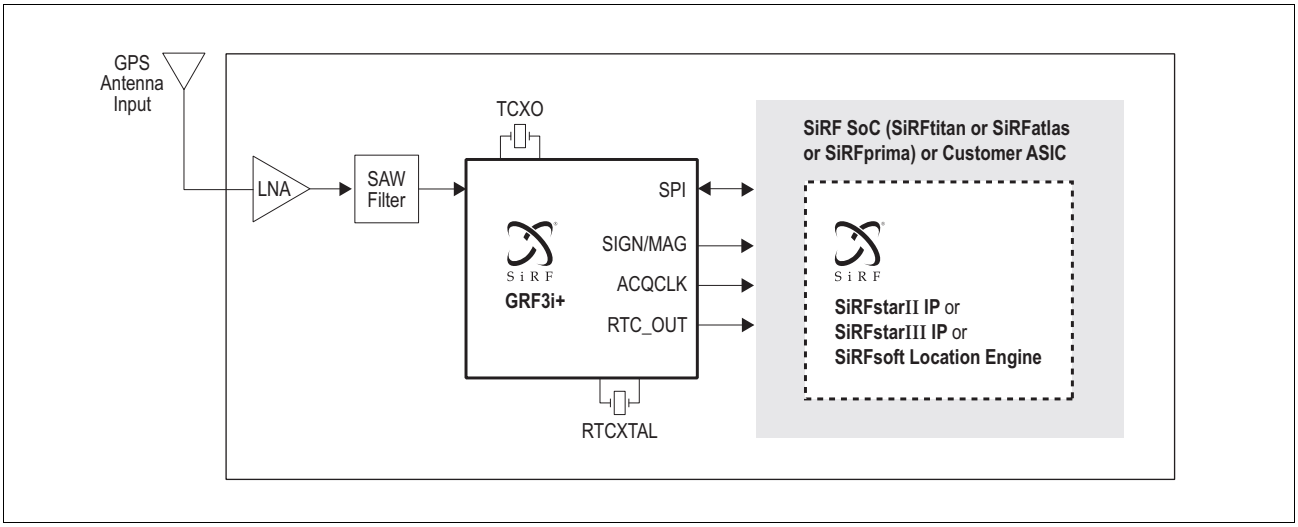


Figure 1. Sample Architecture Diagram

GRF3i+ Description

The GRF3i+ is the latest generation of low power GPS RF front-end devices from SiRF. The GRF3i+ is the first RF chip that is designed to be compatible with the SiRFstarII and SiRFstarIII baseband chip and IP cores, the SiRFsoft GPS signal processing engine, and the SiRF family of System on Chip (SoC) solutions. The GRF3i+ is only available as a companion RF chip to SiRF products, and is not sold as a stand-alone RF chip for non-SiRF solutions.

SIGN and MAG Bit Handling

In SiRF baseband and SiRFsoft modes, the SIGN and MAG data samples are multiplexed onto a single pin.

In SiRF baseband mode, the 2-bit SIGN/MAG sample data is created using a 16 f_0 sample clock. In SiRFsoft mode, the sample data rate and the number of data bits is configurable, which allows the effective data rate to be controlled within the constraints of the host baseband processor interface.

In the SiRF SoC mode of operation, the SIGN and MAG bits are output on separate device pins at a sample rate of 16 f_0.

Core RF Design

The GRF3i+ is designed in the new IBM 7WL 0.18 μm SiGE BiCMOS process and improves upon its predecessor, the GRF3i. The GRF3i+ also incorporates tighter design specifications on each sub-block to achieve an overall improved device specification.

In particular, gain stability over temperature is greatly improved, which allows a greater AGC range for noise suppression and external front end gain variations. The 1 dB compression is improved by 5 dB, which improves system performance in the presence of strong in-band interference. The noise figure of the device is reduced from the typical 9 dB in the previous generation, to approximately 6 dB. An external LNA is still required for best system sensitivity.

Weak Signal Performance Enhancements

A major hurdle in achieving acceptable weak signal performance is overcoming interference from spurious signals in the GPS band. When GPS was a stand-alone sensor application, only external interference sources usually impacted GPS performance. Now GPS is being integrated into many new devices, many of which provide a host of potential interference sources, from discrete spurious signals to higher levels of broadband noise. At a conventional GPS signal level of -130 dBm, spurious noise within the GPS RF channel is not a major concern. With the advent of high-sensitivity GPS and Assisted GPS, where acquisition and tracking of GPS signals is in the range of -155 dBm to -160 dBm, excess noise floor can be a critical limiting factor in achieving optimum performance.

The GRF3i+ incorporates the following three new features to improve overall system performance in high noise environments.

Dual Mode IF Filter

The GRF3i+ incorporates a dual-mode IF filter design. The wide mode provides the IF filter bandwidth of 6 MHz used in previous designs and supports both GPS and Galileo signals. The narrow mode provides a 2 MHz bandwidth setting and a steeper filter cutoff for improved rejection of unwanted signals.

Fractional-N Synthesizer

The GRF3i+ also incorporates a high resolution Fractional-N synthesizer as an improvement over the N/R integer divide in the GRF3i. The Fractional-N improves device frequency selectivity and allows optimum divider settings for different reference frequencies. The GPS LO can therefore be tuned with high precision to address compatibility and interoperability issues in integrated systems.

Power Regulation

The GRF3i+ uses an internal core voltage of 1.8 Vdc, which is supplied by an on-chip regulator This provides ultra-clean power supply for high-sensitivity applications. The GRF3i+ is the first stand-alone GPS RF chip from SiRF to incorporate the regulator into silicon. In addition to the obvious benefit of eliminating an external voltage regulator, the on-chip regulator reduces the dependency of the GRF3i+ on clean power supplied from the host system. Issues such as frequency pulling/pushing and other effects related to instability of the DC voltage are no longer a major concern, which makes the GRF3i+ much easier to integrate.

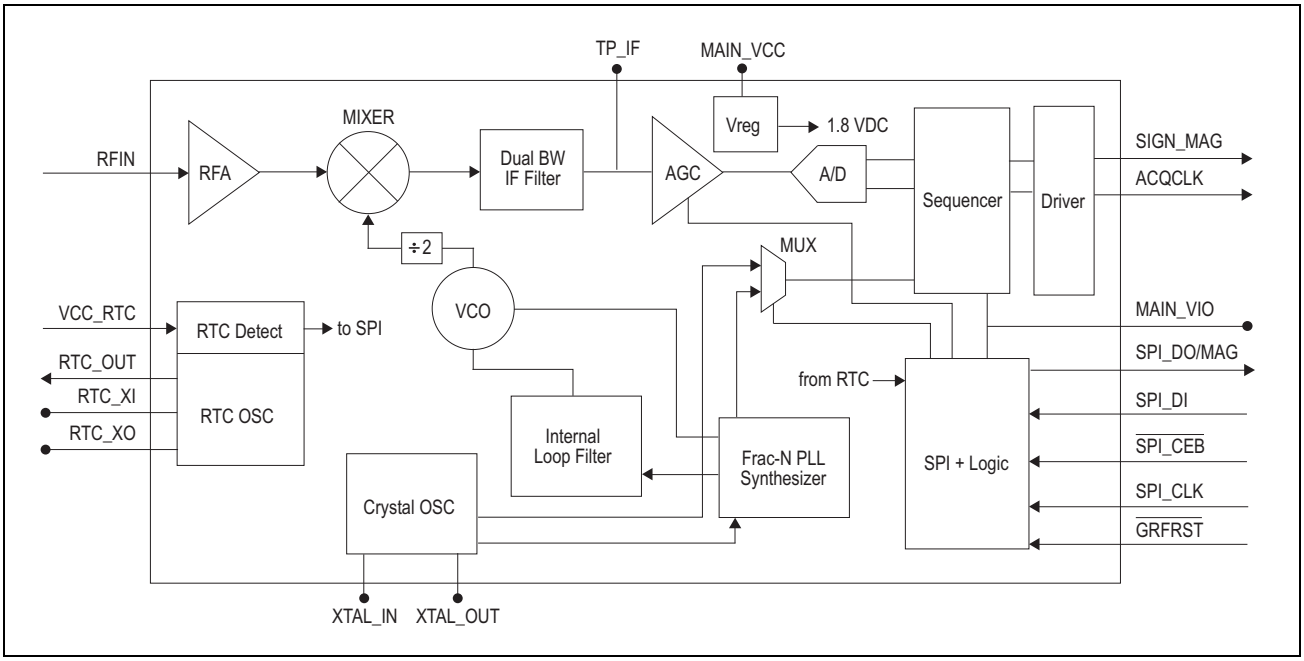


Figure 2. GRF3i+ Internal Block Diagram

FUNCTIONAL DESCRIPTION

RFA

The GRF3i+ receives the GPS L1 signal via an external active or passive antenna. The L1 input signal is a Direct Sequence Spread Spectrum (DSSS) signal at 1575.42 MHz with a 1.023 Mbps Bi-Phase Shift Keying (BPSK) modulated code. Because the input signal power at the antenna is nominally -130 dBm (spread over 2 MHz), the desired signal is below the thermal noise floor. With a front-end input compression point of -65 dBm, rejection of large out-of-band signals is possible given filtering in the IF section. The RFA uses a single-ended RF input for ease of use.

Image-Reject Mixer

The image-reject mixer is a double-balanced design, which significantly reduces common mode interference. The Image-Reject Mixer block also contains an I-Q phase shift combiner. This circuit properly phase shifts and sums the I and Q outputs internal to the image reject mixer to a single channel and achieves an RF image suppression in excess of 25 dB. By using an image-reject mixer, an inexpensive pre-select RF filter may be used. The mixer and on-chip 1571.424 MHz LO produce an IF center frequency of 3.996 MHz.

Dual Bandwidth IF Filter

An IF filter is required between the Mixer and AGC amplifier to provide an anti-aliasing function before A/D conversion. The GRF3i+ incorporates a dual mode IF filter with bandwidth settings of 6 MHz (wide) and 2 MHz (narrow). The narrow IF filter may prove useful in rejecting unwanted signals in certain applications and environments. In the GRF3i+, the IF filter is integrated on-chip, thus minimizing the number of external parts on the board. The IF filter self-calibrates to optimize performance.

This filter typically provides >20 dB roll-off at the alias frequency (located at FS-FIF, where FS is the ADC sample rate), which makes the contribution of C/N_0 degradation due to Nyquist noise folding insignificant. Thus, the combined effect of IF noise aliasing and RF image conversion have a negligible impact to C/N_0 performance.

AGC Amplifier and Control Block

The AGC amplifier provides the additional gain needed to meet the signal range of the 2-bit A/D Converter. The AGC IF gain is digitally controlled by an AGC Control block, which loads and registers digital gain setting words from SiRF GPS baseband engine through the four wire SPI interface. The 5-bit AGC Control register allows

the system to compensate for roughly 50 dB variation in system gain for all causes including temperature, front end configuration, and process variations. The AGC also allows the system to compensate for high noise into the GPS RF front end, such as that due to external jammers and other interference sources. The AGC can also be operated in a self-contained, closed loop mode within the GRF3i+ chip. This mode supports compatibility with SiRF SoCs.

A/D Converter

The AGC amplifier output drives a 2-bit A/D Converter that provides sign and magnitude output bits to the Interface block. The combination of 2-bit quantization and oversampling provides significant improvement in C/N_0 and CW jamming immunity over 1-bit systems.

Sequencer

The sequencer block provides an on-chip decimation function, which may be useful to lower GPS data rates in SiRFsoft-based systems.

RTC Oscillator

This circuit is designed to drive a 32.768 KHz crystal. This oscillator is operational during the sleep cycle of the GRF3i+. The oscillator is specifically designed using a pseudo-inverter topology that provides sufficient gain to start oscillation of the crystal with minimum startup time and minimum current consumption. The crystal is connected between the input and output of this inverter.

An internal differential stage followed by a series of inverters is included to convert and drive the oscillation amplitude to CMOS levels. The RTC oscillator circuit also includes startup circuitry for the bias section to guarantee fast and reliable startup. The RTC provides a 32.768 KHz buffered output to the GPS baseband on the RTC_OUT pin.

Driver

This CMOS driver can drive a capacitive load of up to 10 pF. The driver CMOS output swing is controlled and adjusted by the MAIN_VIO. For SiRF Baseband mode of operation, the SIGN/MAG and ACQCLK signal sample data interface to the baseband conforms to waveform timing diagram shown in Figure 3. For SiRF SoC mode of operation, the SIGN, MAG, and ACQCLK interface conforms to the wave form timing diagram shown in Figure 4.

RTC Detector

During sleep mode, special circuitry is used to monitor the output of the RTC oscillator and indicate the status of the RTC clock upon request from the baseband after the chip is back in normal operation. If during the sleep mode the RTC oscillator output has been lost for at least ten clock cycles, the GRF3i+ flags the baseband via the SPI that the RTC clock is not valid. This feature guards against failure due to temporary disconnection of the crystal, lowering of the supply voltage below the functional level, or temporary loss of power.

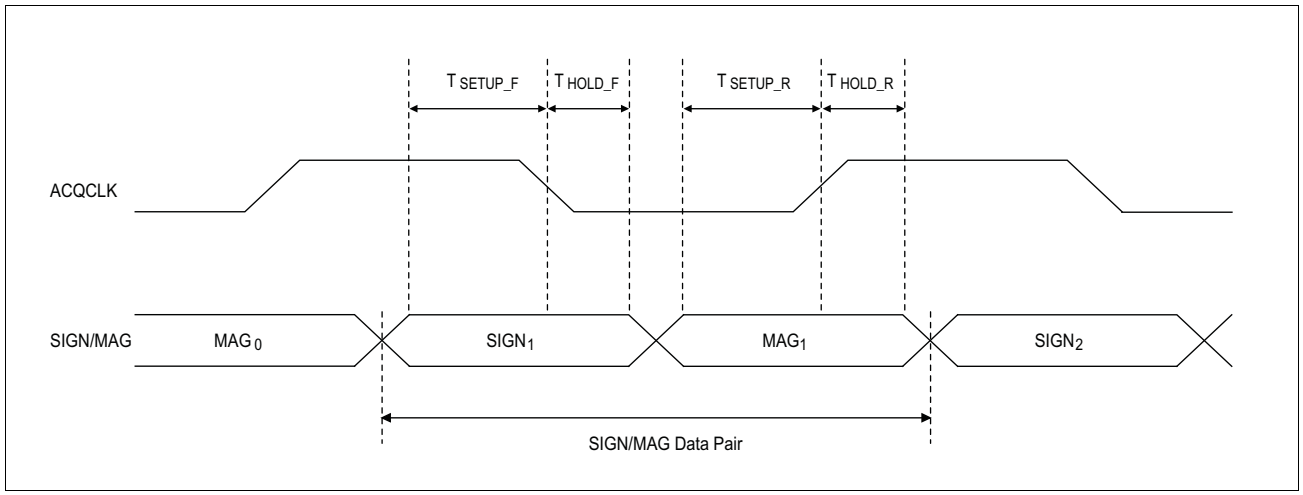


Figure 3. SIGN/MAG and ACQCLK Timing Diagram, SiRF Baseband Mode

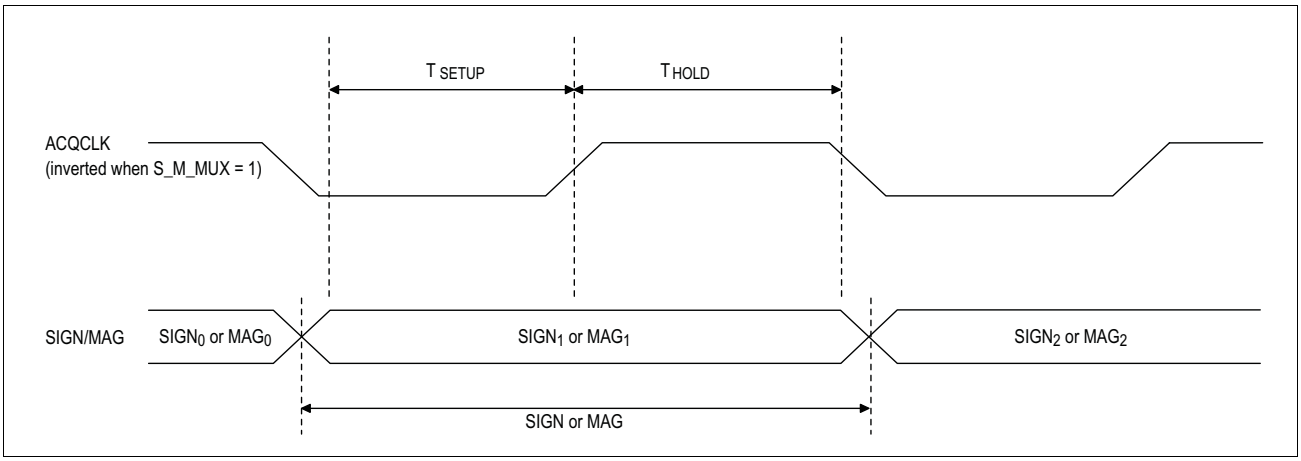


Figure 4. SIGN/MAG and ACQCLK Timing Diagram, SiRF SoC Mode

Reference Oscillator

The Reference Oscillator circuit is designed to accept a 13.0 MHz to 26.0 MHz crystal. However, optimal performance is achieved using a TCXO over the range of 13.0 MHz to 38.4 MHz. The main section is specially designed using a pseudo-inverter topology that provides sufficient gain to start oscillation of the crystal with minimum startup time and minimum current consumption. The crystal is connected between the input and output of this inverter. An internal gain stage followed by a series of inverters is included to convert and drive the oscillation amplitude to CMOS levels. The reference oscillator circuit also includes a startup circuitry for the bias section to guarantee fast and reliable startup.

Frequency Synthesizer

The GRF3i+ GPS down-converter includes a Fractional-N synthesizer that allows the use of a wide range of reference oscillators. The synthesizer generates the local oscillator signal for the image-reject mixer and also generates the ACQCLK.

Internal Loop Filter

An internal loop filter is implemented in GRF3i+ to reduce pin count and improve noise immunity on the control node of the VCO. The GRF3i+ loop filter synthesizer is an on-chip RC filter.

Synthesizer Programming

The list of supported reference oscillator frequencies is shown in the table below.

F_{ref} (MHz)	Mode
13.0	Frac
16.367667	Frac
16.369	Integer
16.8	Frac
19.2	Frac
19.5	Frac
24.5535	Integer
26.0	Frac
33.6	Frac
38.4	Frac

The local oscillator and sample clock (ACQCLK) are derived from an on-chip PLL synthesizer block. The VCO, dividers and phase detector are provided in the chip.

Clock_Mux

This circuit is designed to select between two input frequencies (oscillator and PLL). To avoid glitches, the transition is made by forcing the output low until the switch is completed. The selection of the clock is programmed through the SPI interface. A set of latches along with the supporting gates are used to avoid glitches at the output. Special circuitry enables glitchless transitions between different clock inputs.

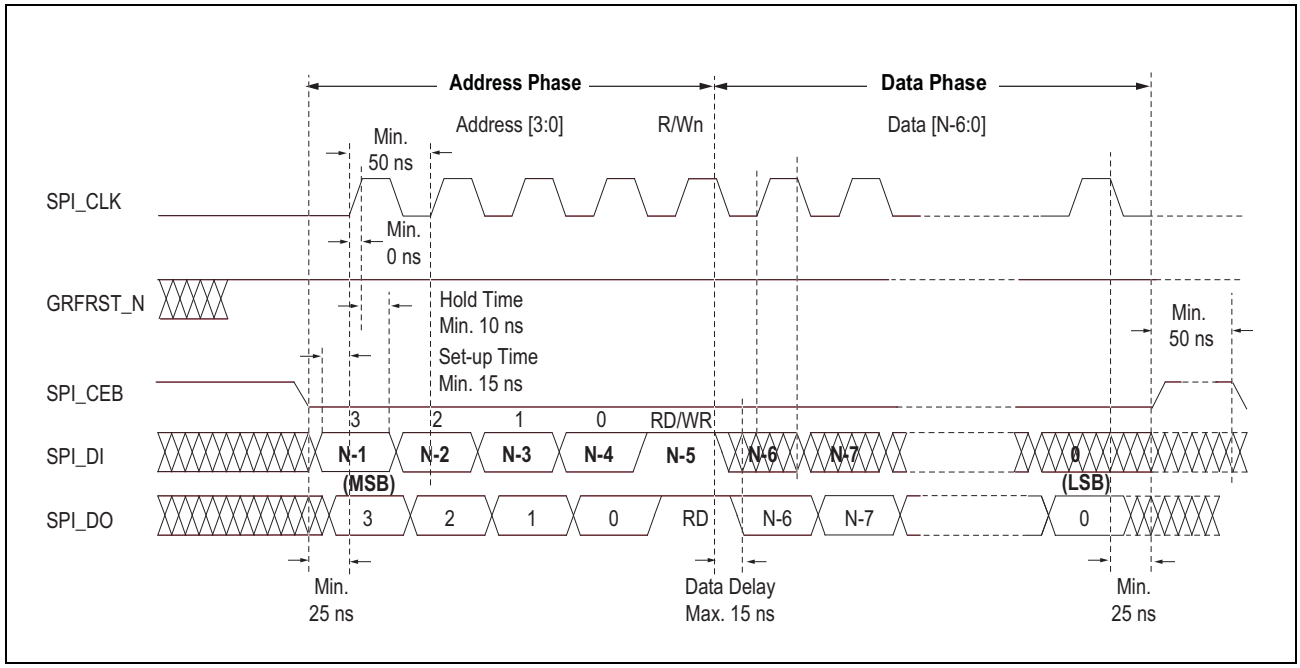
Internal Voltage Regulator

The GRF3i+ provides an internal LDO voltage regulator that regulates the external 2.6 Vdc to 3.6 Vdc supply voltage on the MAIN_VCC to the 1.8 Vdc required by the core RF blocks. The 1.8 Vdc output is provided on the VCC_VCO pin 3. This pin must be externally connected to the remaining VCC pins on the PCB. An external bypass capacitor is required to maintain stability.

The GRF3i+ may also be operated in regulator bypass mode. In this configuration, the 1.8 Vdc core voltage is directly supplied to the individual VCC pins, and the MAIN_VCC supply input to the internal LDO is not connected.

SPI Interface

The SPI port handles communication between the SiRF baseband or host processor and the GRF3i+ for operations such as reference frequency selection, synthesizer programming, AGC setting, IF bandwidth selection, and power control. The GRF3i+ operates in slave mode and can only be controlled by the baseband using SiRF software. The SPI port consists of four pins; SPI_CLK, SPI_DI, and SPI_CEB are inputs, and SPI_DO is an output. The SPI port Read and Write timing configurations are shown in Figure 5.



Note: SPI DI address Read/Write denoted as Bit N-5 is active high for Read and active low for Write.

Figure 5. Read N-bit Message Timing

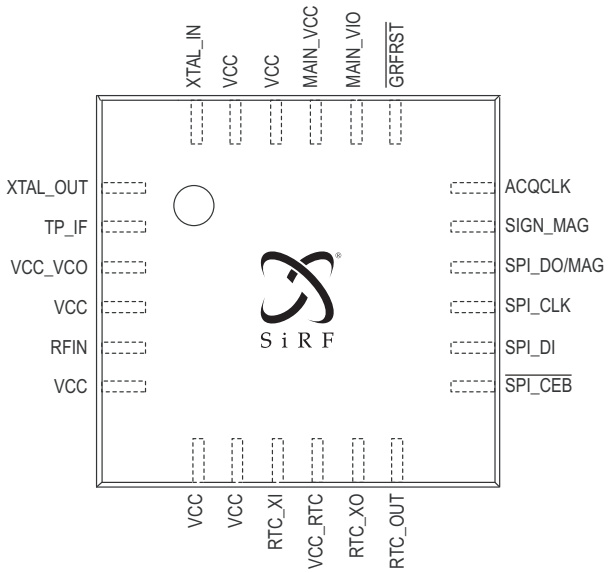


Figure 6. QFN24 Pin Configuration Diagram

PIN DESCRIPTION

Table 1. GRF3i+ Pin Descriptions

Pin #	Symbol	I/O	Description
1	XTAL_OUT	Output	Crystal oscillator output: Use only when a crystal network is placed between this output and the XTAL_IN input in lieu of an external oscillator
2	TP_IF	Output	Analog IF test point controlled via SPI interface
3	VCC_VCO	Supply	Bypass pin. VCO supply pin and internal LDO 1.8 Vdc output must be connected to other VCC pins on PCB
4	VCC	Supply	Bypass pin. Connect to VCC_VCO
5	RFIN	Input	RFA input; GPS RF signal input. Must be AC coupled
6	VCC	Supply	Bypass pin. Connect to VCC_VCO
7	VCC	Supply	Bypass pin. Connect to VCC_VCO
8	VCC	Supply	Bypass pin. Connect to VCC_VCO
9	RTC_XI	Input	RTC crystal oscillator input; a crystal network may be placed between this output and the RTC_XO input in lieu of using an external oscillator
10	VCC_RTC	Supply	Back-up battery supply; must be properly bypassed
11	RTC_XO	Output	RTC crystal oscillator output; a crystal network may be placed between this output and the RTC_XI input in lieu of using an external oscillator
12	RTC_OUT	Output	RTC crystal oscillator buffered output
13	$\overline{\text{SPI\_CEB}}$	Input	SPI interface chip enable

Table 1. GRF3i+ Pin Descriptions *(Continued)*

Pin #	Symbol	I/O	Description
14	SPI_DI	Input	SPI interface data input
15	SPI_CLK	Input	SPI interface clock
16	SPI_DO/MAG	Output	SPI interface data output. MAG bit in SiRF SoC mode.
17	SIGN_MAG	Output	SIGN and MAG combined output in SiRF Baseband mode. SIGN bit only in SiRF SoC mode.
18	ACQCLK	Output	ACQCLK output
19	$\overline{\text{GRFRST}}$	Input	Reset input signal. Must be asserted for 100 msec after power up.
20	MAIN_VIO	Supply	Supply to external I/O section
21	MAIN_VCC	Supply	Main power supply input
22	VCC	Supply	Bypass pin. Connect to VCC_VCO
23	VCC	Supply	Bypass pin. Connect to VCC_VCO
24	XTAL_IN	Input	Reference oscillator (TCXO) input; a crystal network may be placed between this output & the XTAL_OUT input in lieu of an external oscillator
Paddle	GND	Input	Ground reference beneath package

Notes:

1. All VCC pins must be bypassed to ensure reliable operation.
2. Good RF design practices must be adhered to in the PC board layout.
3. A ground plane and a power plane must be used to obtain good performance.

ELECTRICAL SPECIFICATIONS

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Table 2. Absolute Maximum Ratings

Parameter	Rating
Maximum Supply Voltage	3.6 V
Maximum RF Input (no damage)	+10 dBm
Minimum Voltage on Any Pin	GND -0.5 V
Maximum Voltage on Any Pin	3.6 V
Storage Temperature	-65° C to +150° C

Warning – Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 3. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	MAIN_VCC MAIN_VIO VCC_RTC	2.6 1.71 1.4	2.85 2.85 1.5	3.6 3.6 1.6	V
Operating Temperature		-40	-	+85	°C
External Reference Amplitude (when driven externally, XTALIN must be ac-coupled)		500	-	1800	mVpp
External Reference Frequency		13	-	38.4	MHz
RTC Input Voltage		200	400	1800	mVpp
LDO Output Voltage	VCC_VCO	1.71	1.8	1.89	Vdc

Warning – Electrostatic Discharge (ESD) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the GRF3i+ features proprietary ESD protection circuitry to a minimum of 2000 V on all pins permanent damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DC CHARACTERISTICS

All specifications under conditions TOPR = 25° C, VCC = 2.85 V.

Table 4. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Total Supply Current						
Sleep Mode	I_{CC}		0.006	0.01	mA	RTC circuit domain is powered ON. MAIN_VCC and MAIN_VIO are OFF. All circuits off via SPI command.
Normal Mode (Integer)			14.0	16.0		Full power (Integer mode)
Normal Mode (Frac)			16.0	18.0		Full power (Frac-N mode)
Stand-by Mode (Clock Only)			1.5	2.0		ACQCLK and RTC_OUT only
Low Power Mode (Integer)			11.0	12.0		Full power functionality with noise figure increased to 9 dB and gain lowered by 7 dB typical
SPI and RTC Characteristics						
SPI and RF Block CMOS Input High Level	V_{IH}	0.7 * MAIN_VIO			V	
SPI and RF Block CMOS Input Low Level	V_{IL}			0.3 * MAIN_VIO		
SPI and RF Block CMOS Output High Level	V_{OH}	0.8 * MAIN_VIO				
SPI and RF Block CMOS Output Low Level	V_{OL}			0.2 * MAIN_VIO		
RTC Block Output High Level		0.75 * VCC_RTC				
RTC Block Output Low Level				0.25 * VCC_RTC		

Table 5. Thermal Characteristics

Parameter	Symbol	Typ	Unit	Conditions
QFN24 Thermal Resistance Junction-to-Ambient	θ_{JA}	40	°C/W	
Power Supply Current Temperature Coefficient	$\frac{(\Delta Icc/Icc)}{\Delta T}$	0.2	%/°C	

AC CHARACTERISTICS

All specifications under conditions TOPR = 25° C, MAIN_VCC = 2.85 V.
All RF measurements are made with appropriate matching to the input or output impedance.

Table 6. AC Characteristics

AC Characteristic	Symbol	Min	Typ	Max	Unit	Conditions
RFA/Mixer/AGC						
Noise Figure (AGC @ min. Gain) Normal Mode			6.0	9.0	dB	Normal mode, integer
Noise Figure (AGC @ min. Gain) Low Power Mode	NF		9.0	12.0		Low power mode, integer
Input 1 dB Gain Compression (AGC @ min. Gain) Normal Mode	IP_{1db}	-65	-60		dBm	At RFA input
Input 1 dB Gain Compression (AGC @ min. Gain) Low Power Mode		-60	-55			
Input Return Loss	S11	8	10		dB	
Image Rejection Ratio (AGC @ typ. Gain)		25	30			
Frequency Synthesizer						
VCO Operating Frequency SiRF Baseband SiRF SoC			 3142.848 3142.592		MHz	Low side injection. LO = F_{VCO} ÷ 2.
Type of Synthesizer		Frac-N				
Reference Frequency		13		38.4	MHz	10 discrete frequencies
Reference Input Level		500		1800	mVpp	Crystal oscillator
LO SSB Phase Noise @ 1.0 Hz @ 10 Hz @ 150 Hz @ 1.0 kHz @ 10 kHz > 10 kHz to 3 MHz				 -24 -54 -74 -80 -80 -90	dBc/Hz	
Local Oscillator Discrete Spurious 0.1 to 10 Hz 10 Hz to 100 Hz 100 Hz to 10 KHz 10 KHz to 40 MHz				 -15 -40 -40 -30	dBc	LO frequency = 1571.42 MHz
VCO Leakage			-70	-50	dBm	RF input pin
IF Filter/AGC-AMP						
IF Center Frequency SiRF Baseband Mode SiRF SoC Mode	Fc		 3.996 4.12397		MHz	
Filter 3 dB Bandwidth Wide Filter Narrow Filter	BW	 5.4 1.7	 6.0 2.0	 6.6 2.3		3 dB bandwidth
IF Rejection Wide Filter, Fc + 4 MHz Wide Filter, Fc + 8 MHz Narrow Filter, Fc ± 3 MHz Narrow Filter, Fc + 8 MHz		 10 20 50 80	 15 50 55 85		dB	Stopband Attenuation
Voltage Gain Resolution			1.7			5 bits
Gain Adjust Range		45	50			
Minimum Receiver Gain		44	50			
Maximum Receiver Gain			100	102		

Table 6. AC Characteristics *(Continued)*

AC Characteristic	Symbol	Min	Typ	Max	Unit	Conditions
CMOS Driver						
Rise time @ 10 pF Load (10% to 90%)			4.0		ns	
Fall time @ 10 pF Load (90% to 10%)			4.0			
SPI Interface Timing (Read/Write Mode)						
Set-up Time	T_S	15			nsec	See Figure 5.
Hold Time	T_H	10				
SPI Clock Frequency	SPI_CLK		4	20	MHz	
RF Interface Timing (SIGN/MAG and ACQCLK)						
Set-up Time	T_{SETUP}	5			nsec	See Figure 3. and Figure 4.
Hold Time	T_{HOLD}	5				
Acquisition Clock SiRF Baseband Mode SiRF SoC Mode	ACQCLK		 16.369 16.367667		MHz	

SAMPLE CIRCUIT FOR GRF3I+

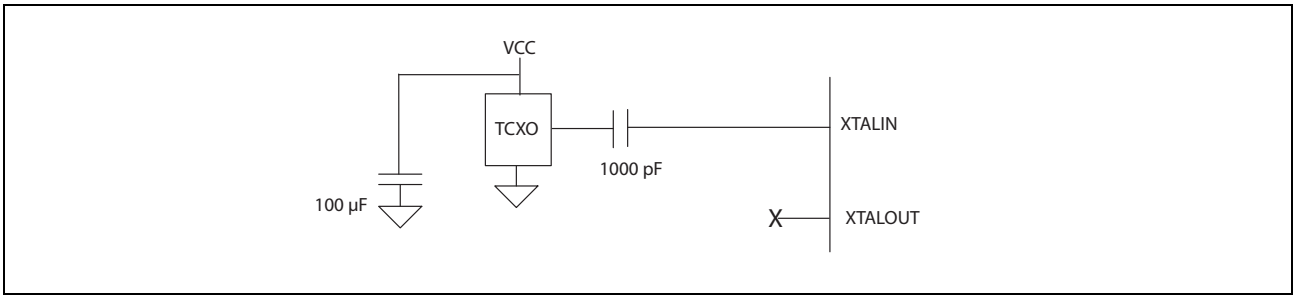


Figure 7. Typical TCXO Circuitry (16.369 MHz)

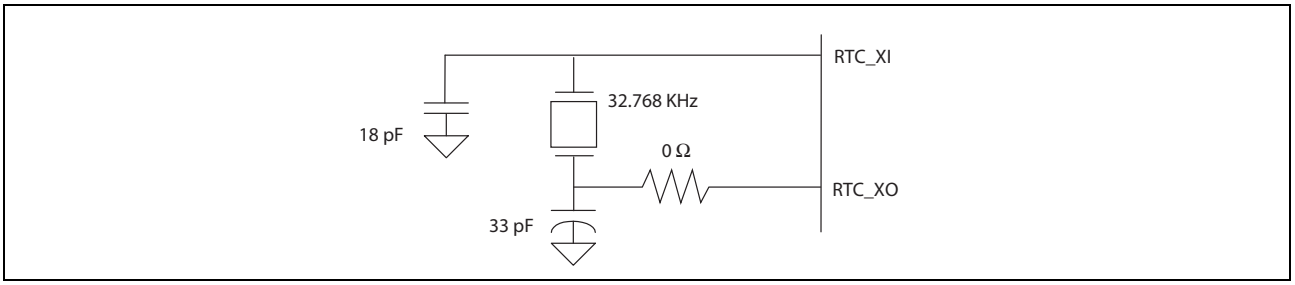


Figure 8. Typical RTC Circuitry

Figure 9. Typical RFIN Input Impedance Matching Circuitry

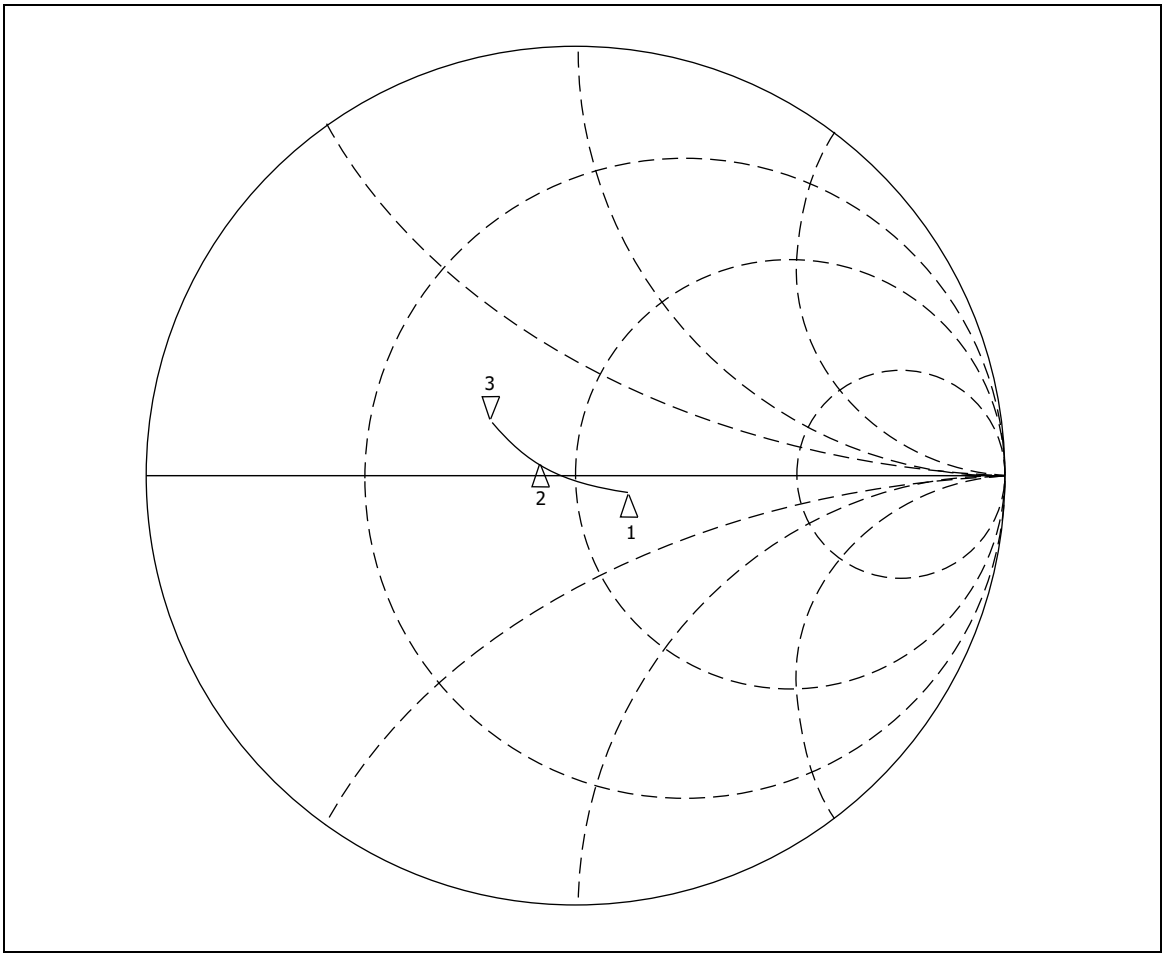


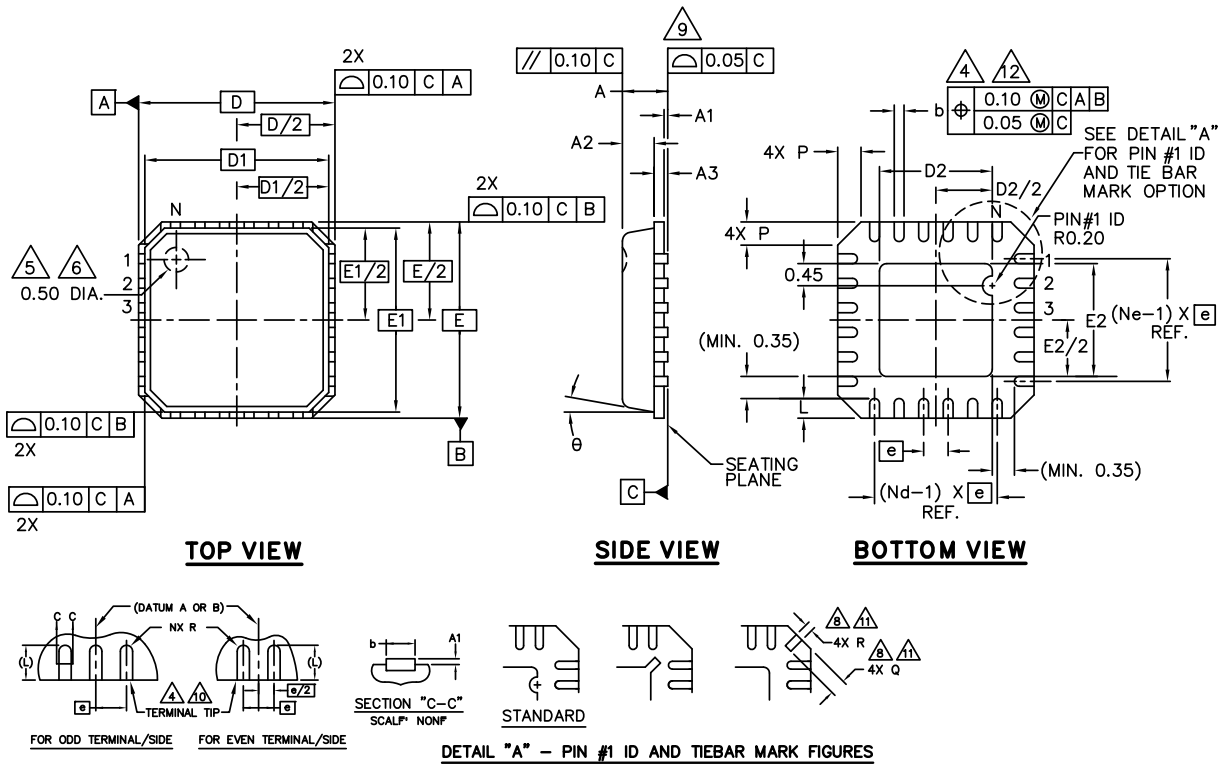
Figure 10. RFA Input Impedance Smith Chart for 24 Pin-QFN

Table 7. RFA Input Impedance Over Frequency (S11)

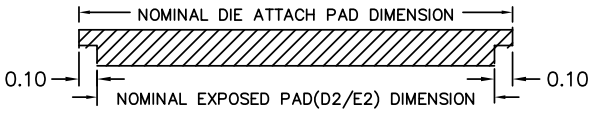
Test Conditions: RF Input = -60 dBm, Zo = 50 Ω, 2.85 V, 25° C.

Marker	1	2	3
Frequency	1475 MHz	1575 MHz	1675 MHz
Impedance	63.55 - j 5.58 Ω	41.79 + j 2.40 Ω	32.45 + j 8.70 Ω

MECHANICAL SPECIFICATIONS



GENERAL ; NOMINAL EXPOSED PAD(D2/E2) DIMENSION = NOMINAL DIE ATTACH PAD DIMENSION−0.20



<DIE ATTACH PAD X−SECTION VIEW>

SYMBOLS	D2			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED PAD VARIATIONS	2.40	2.50	2.60	2.40	2.50	2.60

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. − 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X−DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y−DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
10. APPLIED ONLY FOR TERMINALS.
11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
12. FOR 0.40 mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07 mm AT THE ACTUAL MEAN VALUE OF BODY SIZE.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	10
A2	0.60	0.65	0.70	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ	0	−	12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	8,11
R	0.13	0.17	0.23	8,11

SYMBOL	PITCH VARIATION E			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		24		3
Nd		6		3
Ne		6		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4,12
D2	SEE EXPOSED PAD VARIATION: B,C,D,E			
E2	SEE EXPOSED PAD VARIATION: B,C,D,E			

Figure 11. GRF3i+ QFN24 Package

Ordering Information

Part Number	Description
GRF3i-0336	GRF3i+, QFN-24, Lead Free

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