SiRFFlash User Guide

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SiRFFlash User Guide

About This Document

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Getting Help

If you have any problems with your product, contact your SiRF representative or call or send an email to the SiRF Technology support group:

Phone +1 (408) 467-0410

Email support@sirf.com

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Preface

The *SiRFFlash User Guide* explains how to install and use SiRFFlash™, a flash memory programming and reading utility. GPS receiver boot mode options and other programming considerations are also covered, along with troubleshooting messages.

This User Guide is based on SiRFFlash release version 3.40, but may be relevant to later versions.

Who Should Use This Guide

This manual was written assuming the user has basic computer skills and is familiar with the Windows operating environment.

How This Guide Is Organized

Chapter 1, "Overview" provides a brief overview of SiRFFlash features, architecture, and system requirements.

Chapter 2, "Installation" gives detailed information on how to install SiRFFlash and connect the GPS receiver.

Chapter 3, "Using the SiRFFlash Graphical Interface" provides detailed instructions for operating SiRFFlash software through the GUI interface.

Chapter 4, "Using SiRFFlash Command Line" provides detailed instructions for operating SiRFFlash software by the use of the command line option.

Chapter 5, "Flash Programming Considerations" details input file formats and communication settings, such as bus widths and Baud rates, and other types of flash memory.

Chapter 6, "Receiver Boot Mode" describes how to place various SiRF Evaluation Receivers and Development Boards in the appropriate boot mode needed for SiRFFlash operation.

Appendix A, "Troubleshooting" provides additional information about error messages that are generated when programming errors occur.

Appendix B, "Serial Peripheral Interface Support" provides additional information about SiRFFlash support for Serial Peripheral Interface (SPI).

Appendix C, “Acronyms and Abbreviations Glossary” describes the terms used in this manual and others.

Contacting SiRF Technical Support

Address:

SiRF Technology Inc.
217 Devcon Drive
San Jose, CA 95112 U.S.A.

SiRF Technical Support:

Phone: +1 (408) 467-0410 (9 am to 5 pm Pacific Standard Time)
E-mail: support@sirf.com

General enquiries:

Phone: +1 (408) 467-0410 (9 am to 5 pm Pacific Standard Time)
E-mail: gps@sirf.com

Helpful Information When Contacting SiRF Technical Support

Receiver Serial Number: _____

Receiver Software Version: _____

SiRFFlash Version: _____

Overview 1

SiRFFlash is a fast in-circuit flash memory programming and reading utility designed to support the SiRF® Technology SiRFstarII and SiRFstarIII family of chip sets. In addition to supporting a variety of flash chips from leading manufacturers, it also supports multiple input file formats.

SiRFFlash can be used to program and read flash memory on a SiRFstarII or SiRFstarIII based Evaluation Receiver, Development Board, or other SiRF-based GPS products.

SiRFFlash architecture is comprised of three main components:

- A graphical user interface (GUI)
  A GUI version of SiRFFlash for quick-and-easy operation.
- A command line console application (SiRFflashcl.exe)
  A flexible command line driven SiRFFlash engine.
- A chipset list (chiplist.txt)
  An extensive flash memory chip list offering add-on capability.

Required Hardware

The following is the minimum hardware that is required to run SiRFFlash:

- A PC running Windows 98 or later
- One available RS232 serial port or one available USB port
- A serial connector, such as wire, USB to serial, or Bluetooth interface

Note – SiRFFlash can also be run using serial peripheral interface (SPI). Refer to Appendix B, “Serial Peripheral Interface Support” for more information about SPI.

Supported Input File Formats

The SiRFFlash program supports four input file formats:

- Motorola S record (typical extension “.s”)
- Intel Hex (typical extension “.hex”)
- Binary (typical extension “.bin”)
- Arm Executable File (typical extension “.axf”)

Installation 2

This chapter provides instructions for installing the SiRFFlash software as well as connecting the required hardware.

Installing SiRFFlash

The method of installing SiRFFlash depends on how SiRFFlash is obtained—either from a CD included with a toolkit (Evaluation Kit or System Development Kit), or downloaded from the SiRF *Customer Zone*.

To install SiRFFlash from a toolkit CD:

1. Insert the CD in your CD-ROM drive.

   After a few seconds, a CD browser automatically launches and is displayed on your screen.

2. Select Software Tools from the main menu of the browser interface.

3. Select SiRFFlash from the software tool list.

   An install shield guides you through the rest of the installation.

To install SiRFFlash that has been downloaded from the SiRF *Customer Zone*:

1. Extract the `SETUP.EXE` file from the ZIP file.
2. Double click on the file `SETUP.EXE`.

   An install shield wizard guides you through the rest of the installation.

Installing the Hardware

When programming or reading flash memory, the only requirement is a connection between the PC and the GPS receiver via the serial port, which also supports USB and Bluetooth interface.

To install the hardware:

1. Establish a connection between the PC and the GPS receiver

   Connect one end of the serial or USB cable to the PC and the other end to the GPS receiver. If it is a SiRF Evaluation Receiver or Development Board, COM-A should be used.

   SiRFFlash supports USB communication. Before USB can be used however, it is necessary to install the required USB drivers. See “Installing USB Drivers” on page 2-2 for the USB driver installation process.
2. Connect power to the GPS receiver and ensure the receiver is switched on.
3. Place the GPS receiver in internal boot mode.

Note – SiRFFlash supports internal and external boot modes. It is highly recommended to use internal boot mode when possible. For detailed information about placing a GPS receiver in internal boot mode, please see “Placing The GPS Receiver in Internal Boot Mode” on page 6-1.

Installing USB Drivers

SiRFFlash supports USB communication. However, before USB can be used, it is necessary to install the required USB drivers. These drivers were copied to the SiRFFlash directory during the installation process of SiRFFlash. The install process for the USB drivers is different for each Windows operating system.

Note – If USB is being used, the USB port is listed as an additional serial port in the Data Source Setup dialog.

Windows XP Installation

To install the required USB drivers on Windows 2000:

1. Connect the USB enabled SiRF GPS receiver to your PC.

   Windows opens a “Found New Hardware Wizard” window.

2. Select “Install from a list or specific location (Advanced)” and press *Next*.
3. Select “Include this location in the search”.
4. Press *Browse* to locate the directory where the drivers are located and press *OK*.

   The drivers were copied to the SiRFFlash directory during the SiRFFlash installation. By default, the directory is “C:\Program Files\SiRF\SiRFFlash\usbDrivers”
5. Press *Finish* to complete the installation of the “CP2101 USB Composite Device”.

   Windows now opens a second “Found New Hardware Wizard” window.
6. Repeat steps 2 through to 4.
7. Press *Finish* to complete the installation of the “CP2101 USB to UART Bridge Controller”.

Windows 2000 Installation

To install the required USB drivers on Windows 2000:

1. Connect the USB enabled SiRF GPS receiver to your PC.

   Windows opens a “Found New Hardware Wizard” window.
2. Press *Next* to continue.
3. Select “Search for the best driver for your device (Recommended)” and press *Next*.
4. Select “Specify a location” and press *Next*.
5. Press *Browse* and locate the file “slabbus.inf”.

   The drivers were copied to the SiRFFlash directory during the SiRFFlash installation. By default, the directory is “C:\Program Files\SiRF\SiRFFlash\usbDrivers”
6. Press *Finish* to complete the installation of the “CP2101 USB Composite Device”.

   Windows now opens a second “Found New Hardware Wizard” window.
7. Press *Next* to continue and follow steps 2 through to 4.
8. Press *Browse* and locate the file “slabw2k.inf”.
9. The drivers were copied to the SiRFFlash directory during the SiRFFlash installation. By default, the directory is “C:\Program Files\SiRF\SiRFFlash\usbDrivers”
10. Press *Finish* to complete the installation of the “CP2101 USB to UART Bridge Controller”.

Windows 98 Installation

To install the required USB drivers on Windows 98:

1. Connect the USB enabled SiRF GPS receiver to your PC.

   Windows opens a “Found New Hardware Wizard” window.

2. Press *Next* to continue.

3. Select “Search for the best driver for your device (Recommended)” and press *Next*.

4. Select “Specify a location”.

5. Press *Browse* to locate the directory where the drivers are located and press *Next*.

   The drivers were copied to the SiRFFlash directory during the SiRFFlash installation. By default, the directory is “C:\Program Files\SiRF\SiRFFlash\usbDrivers”

6. Press *Finish* to complete the installation of the “CP2101 USB Composite Device”.

   Windows now opens a second “Found New Hardware Wizard” window.

7. Press *Next* to continue and follow steps 2 through to 5.

8. Press *Finish* to complete the installation of the “CP2101 USB to UART Bridge Controller”.

Using the SiRFFlash Graphical Interface 3

SiRFFlash is capable of four main functions:

- Programming flash memory
- Detecting flash memory
- Reading flash memory
- Erasing flash memory

The following sections provide information about how to use the flash memory programming and memory reading functions via the SiRFFlash graphical interface.

Programming Flash Memory

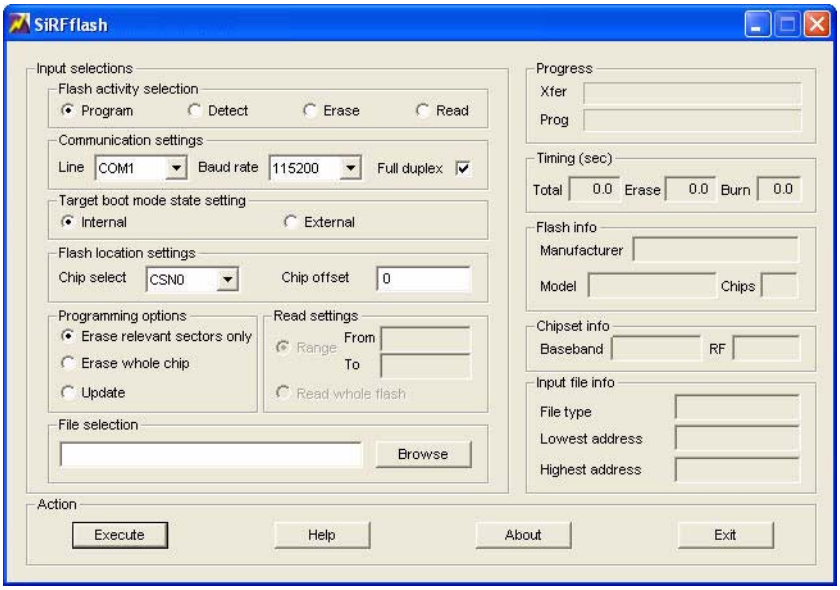
Before attempting to use the flash memory programming function of SiRFFlash, the GPS receiver must be connected to the PC being used, powered, and operating in internal boot mode. For details on installation and boot mode operation, see “Installing the Hardware” on page 2-2 and “Placing The GPS Receiver in Internal Boot Mode” on page 6-1.

The following instructions are provided for basic flash programming.

To program flash memory on a GPS receiver:

1. Start the SiRFFlash software by selecting the SiRFFlash shortcut created during installation in the Start | Programs | SiRF folder.

The SiRFFlash software is launched.



2. Select the *Program* radio button in the *Flash activity selection* group.

3. From the *Communication settings*, *Target boot mode state settings*, and the *Programming options* groups, select the required settings. Table 3-1 provides a description of each option and setting.

Table 3-1 Flash Activity Selection, Communication Settings, Target Boot Mode State Settings, Flash Location Settings, and Programming Options

Parameter	Description
Flash activity selection | Program	Sets SiRFFlash to program flash with the contents of an input file.
Flash activity selection | Detect	Sets SiRFFlash to detect which flash chip is used and which Baseband and RF chips are used.
Flash activity selection | Erase	Sets SiRFFlash to erase entire flash chip.
Flash activity selection | Read	Sets SiRFFlash to read conents of the flash chip and write the contents to a file.
Communication settings | Line	The comm port of the PC that is connected to the GPS receiver.
Communication settings | Baud rate	The Baud rate used during the flash memory programming. It is recommended to use the 115200 Baud rate selection to minimize programming time. See “Communication Settings” on page 5-2 for additional information about Baud rate settings.
Communication settings | Full Duplex	Full duplex should be selected for maximum transmission rate. Half duplex communication is only used in internal boot mode. See “Communication Settings” on page 5-2 for additional information about full duplex settings.

Table 3-1 Flash Activity Selection, Communication Settings, Target Boot Mode State Settings, Flash Location Settings, and Programming Options *(Continued)*

Parameter	Description
Target boot mode state setting | Internal	The GPS receiver is placed in internal boot mode via a toggle switch or other means. It is highly recommended to use internal boot mode when possible. See “Placing The GPS Receiver in Internal Boot Mode” on page 6-1 and “How Boot Mode is Determined at Power On” on page 6-4 for additional information.
Target boot mode state setting | External	SiRFFlash can place the GPS receiver in external boot mode via this setting. However, it is highly recommended to use internal boot mode when possible. See “Placing The GPS Receiver in Internal Boot Mode” on page 6-1 and “How Boot Mode is Determined at Power On” on page 6-4 for additional information.
Flash location settings | Chip select	Refer to “Advanced Options” on page 3-9.
Flash location settings | Chip offset	Refer to “Advanced Options” on page 3-9.
Programming options | Erase relevant sectors only	Programming flash memory is a two step process. First locations that must be written are erased. Then these locations are written to. If *Erase relevant sectors only* is chosen, the minimum number of sectors are erased only. This sometimes results in the fastest flash programming time.
Programming options | Erase whole chip	The whole flash chip is erased. This ensures that all flash bytes that are not programmed have the value 0xff. With some flash chips, this method is faster than erasing relevant sectors only.
Programming options | Update	No sectors are erased, but specified locations are written to. This option is used when appending existing tables, arrays, and other content.

4. Select the input file by typing the file name in the *File selection* field or use the *Browse* button to find and select the required file.

   The only file needed when programming flash memory in a SiRF Evaluation Receiver or Development Board is a Motorola s record (.s) file (GSW2, SiRFXTrac, or GSW3 for example). However, a binary file (.bin), an ARM executable file (.axf), or an Intel Hex file (.hex) may also be used. See “Working with Input Files” on page 5-1 for detailed information.

Note – A Motorola s record (.s) file is an ASCII representation of a binary image.

5. Click on the *Execute* button to start the flash programming process.

   When the download is successfully completed, a window indicating that the programming was successful is displayed.

6. Return the GPS receiver to external boot mode.

   If you set a jumper or switch to place the receiver in internal boot mode, see Table 6-1 for instructions on setting the switch or jumper to external boot mode. If you entered internal boot mode by using a command (such as using the target boot mode state setting | external), simply reset or power cycle the receiver.

Note – It is possible to select the location of the flash memory that is accessed for programming using the *Flash location settings*. This is an advanced option only. Please see "Advanced Options" on page 3-9 for more information.

Detecting Flash Memory

SiRFFlash can detect which flash chip is used and which Baseband and RF chips are used.

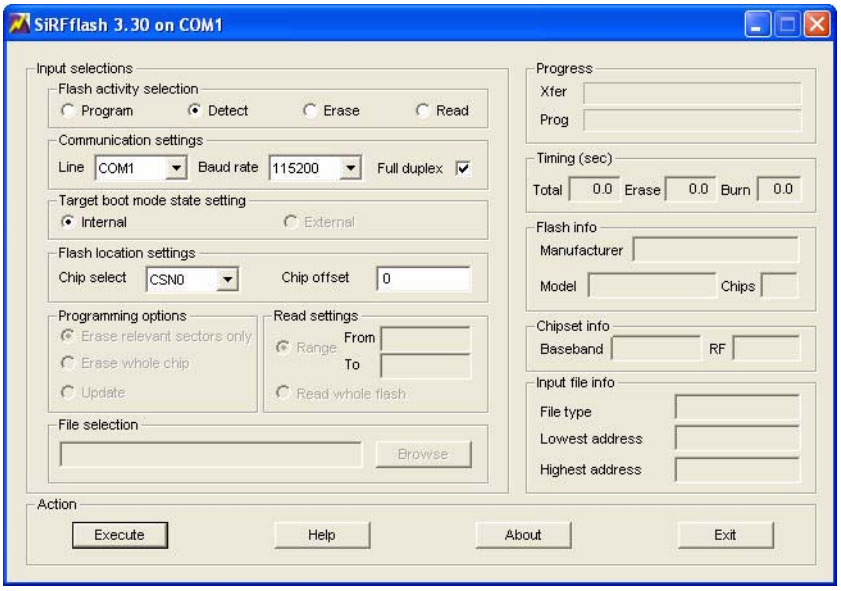
Before attempting to use the flash memory detect function of SiRFFlash, the GPS receiver must be connected to the PC being used, powered, and operating in internal boot mode. For details on installation and boot mode operation, see "Installing the Hardware" on page 2-2 and "Placing The GPS Receiver in Internal Boot Mode" on page 6-1.

The following instructions are provided to detect flash programming.

To detect flash memory on a GPS receiver:

1. Start the SiRFFlash software by selecting the SiRFFlash shortcut created during installation in the Start | Programs | SiRF folder.

   The SiRFFlash software is launched.



2. Select the *Detect* radio button in the *Flash activity selection* group.

   If the SiRFFlash Detect function is successful, a window is displayed.

Reading Flash Memory

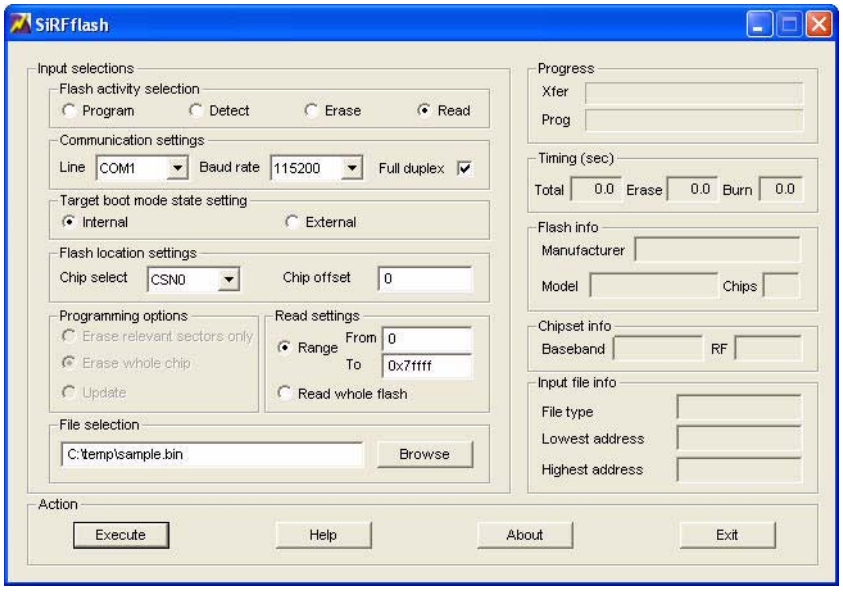
SiRFFlash can read a selected memory address range and write it to a file.

Before attempting to use the read flash memory function of SiRFFlash, the GPS receiver must be connected to the PC being used, powered, and operating in internal boot mode. For details on installation and boot mode operation, see “Installing the Hardware” on page 2-2 and “Placing The GPS Receiver in Internal Boot Mode” on page 6-1.

To read the flash memory of a GPS receiver:

1. Start the SiRFFlash software by selecting the SiRFFlash shortcut created during installation in the Start | Programs | SiRF folder.

   The SiRFFlash software is launched.



2. Select the *Read* radio button in the *Flash activity selection* group.

3. From the *Communication settings*, *Target boot mode state setting*, and the *Read settings* groups, select the required settings. Table 3-2 provides a description of each option and setting.

Table 3-2 Communication Settings and Reading Options

Parameter	Description
Communication settings | Line	The comm port of the PC that is connected to the GPS receiver.
Communication settings | Baud rate	The Baud rate that is used during the read process. It is recommended to use 115200 to minimize operation time.
Communication settings | Full Duplex	Full duplex should be selected for maximum transmission rate. Half duplex communication is only used in internal boot mode. See "Communication Settings" on page 5-2 for additional information about full duplex settings.
Target boot mode state setting | Internal	The GPS receiver is placed in internal boot mode via a toggle switch or other means. It is highly recommended to use internal boot mode when possible. See "Placing The GPS Receiver in Internal Boot Mode" on page 6-1 and "How Boot Mode is Determined at Power On" on page 6-4 for additional information.
Target boot mode state setting | External	SiRFFlash can place the GPS receiver in external boot mode via this setting. However, it is highly recommended to use internal boot mode when possible. See "Placing The GPS Receiver in Internal Boot Mode" on page 6-1 and "How Boot Mode is Determined at Power On" on page 6-4 for additional information.
Flash location settings | Chip select	Refer to "Advanced Options" on page 3-9.
Flash location settings | Chip offset	Refer to "Advanced Options" on page 3-9.
Read settings | From address	Represents the starting address (offset from the start of the flash chip) of the data to be read and stored in the output file.
Read settings | To address	Represents the ending address (offset from the start of the flash chip) of the data to be read and stored in the output file.
Read settings | Read whole flash	Allows reading of entire flash.

4. Type an output file name in the *File selection* field and use the *Browse* button to select a location to save your file. Any file extension can be used although the actual file content is binary (typically .bin is used).

5. Click on the *Execute* button to start the flash reading process.

   SiRFFlash stores the results of the flash reading process in a plain binary file. The value of the first byte in that file is the contents of the memory location whose address is calculated by adding the address corresponding to the chosen *Chip select* and the *Chip offset*, plus *Starting address*.

Note – It is possible to select the location of the flash memory that is accessed for reading using the *Flash location settings*. This is an advanced option only. Please see "Advanced Options" on page 3-9 for more information.

Erasing Flash Memory

SiRFFlash can erase the entire contents of the flash chip.

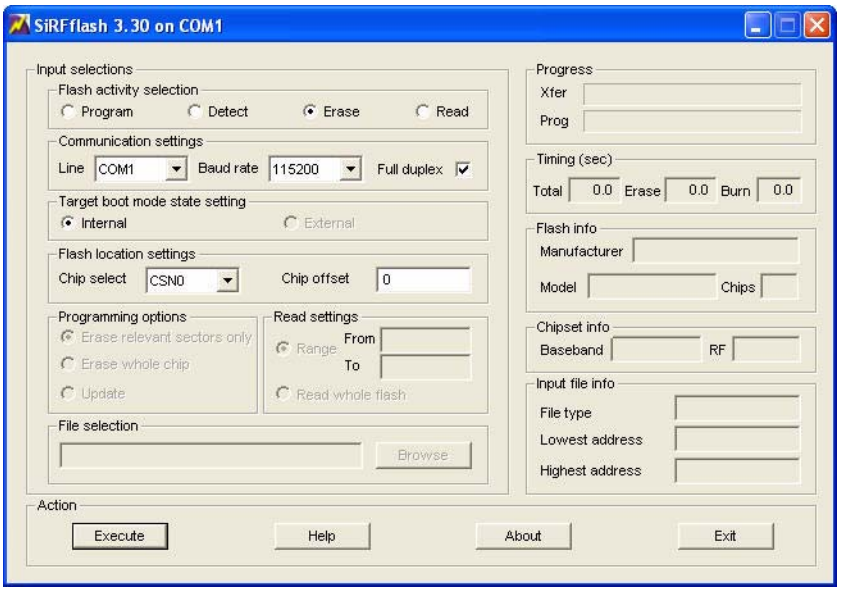
Before attempting to use the erase flash memory function of SiRFFlash, the GPS receiver must be connected to the PC being used, powered, and operating in internal boot mode. For details on installation and boot mode operation, see “Installing the Hardware” on page 2-2 and “Placing The GPS Receiver in Internal Boot Mode” on page 6-1.

The following instructions are provided to detect flash programming.

To erase flash memory on a GPS receiver:

1. Start the SiRFFlash software by selecting the SiRFFlash shortcut created during installation in the Start | Programs | SiRF folder.

The SiRFFlash software is launched.



2. Select the *Erase* radio button in the *Flash activity selection* group.

If the SiRFFlash erase function is successful, a window is displayed.

Displayed Information

During flash programming or reading, SiRFFlash displays information about the progress of the flash memory programming, reading, and the flash memory itself, chipset information, and the input file. This is located on the right side of the SiRFFlash interface.

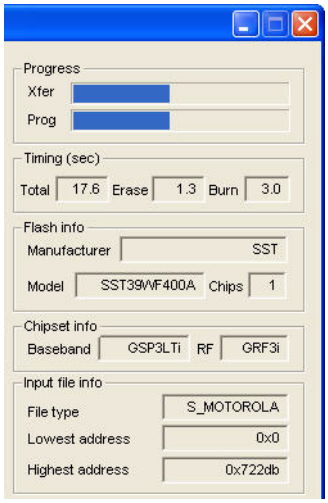


Table 3-3 provides a description of each information field.

Table 3-3 Information Displayed by SiRFFlash

Parameter	Description
Progress | Xfer Progress | Prog	During flash programming, two activities are performed in parallel; data transfer from the PC to the GPS receiver, and the flash programming itself. The *Xfer* field displays the data transfer progress. The *Prog* field displays the flash memory programming progress.
Timing | Total	The total time taken in seconds to program the flash memory.
Timing | Erase	The total time spent performing erase functions during the flash memory programming process.
Timing | Burn	The total time spent performing writing functions during the flash memory programming process.
Flash Info | Manufacturer	The manufacturer code of the flash memory that is being programmed.
Flash Info | Model	The model number of the flash memory that is being programmed.
Flash Info | Chips	The number of individual chips making up the flash memory total that is being programmed. In systems with 16-bit external data bus, the number of chips is one; while in systems with 32-bit external data bus that number is two.
Chipset Info | Baseband	Identifies the baseband chip (such as GSP2 or GSP3) that is being used to access the flash memory.
Chipset Info | RF	Identifies the RF chip (such as GRF2i or GRF3i) that is being used.

Table 3-3 Information Displayed by SiRFFlash *(Continued)*

Parameter	Description
Input File Info | File Type	Identifies the type of file used as input to SiRFFlash: Motorola S record (typical extension ".s") Intel Hex (typical extension ".hex") Binary (typical extension ".bin") Arm Executable File (typical extension ".axf")
Input File Info | Lowest Address	Lowest address programmed by the input file. For binary files, lowest address is always 0.
Input File Info | Highest Address	Highest address programmed by the input file.

Advanced Options

SiRFFlash offers the ability to select the location of the flash memory chip that is accessed for either flash programming or reading. This is controlled by the *Flash location* settings. Table 3-4 provides a description of each of the settings.

Table 3-4 Flash Location Settings

Parameter	Description
Flash location settings | Chip select	Describes which chip select (CSN*x*) on the processor is used to access the flash during programming/reading. Other chip selects (CSN1, CSN2, and so forth) have starting addresses set by internal registers. Defaults are 0x4100 0000 for CSN1, 0x4200 0000 for CSN2, and so forth. If the system is booted in external mode, chip selects are visible at addresses beginning at 0x4000 0000 and 0x0.
Flash location settings | Chip offset	Simpler systems set flash at *Chip offset* 0 in the CSN0 area. In this case, the default value for *Chip offset* (CSN0) must be selected. In more complex systems, multiple flash chips may be within certain CSN*x* areas, in which case, a non-zero *Chip offset* must be selected when access (programming or reading) to those chips is required.

Note – When downloading software to a SiRF Evaluation Receiver, the *Flash location settings* must be left at the defaults of *CSN0* and *0* (zero).

One-Click SiRFFlash Operation

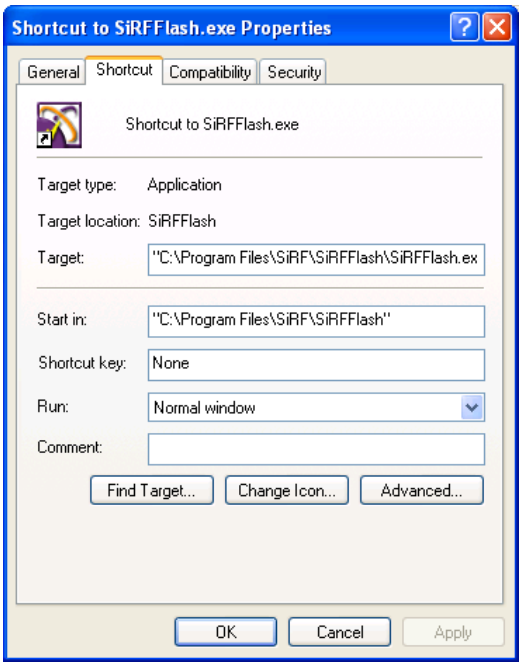
SiRFFlash can be programmed to allow one-click operation. This is useful when one file is programmed multiple times using the same port. To achieve one-click-operation:

1. Create a shortcut to the SiRFFlash executable on your desktop.

Note – The SiRFFlash shortcut icon that appears on the desktop when SiRFFlash is first installed cannot be used to configure one-click SiRFFlash operation. A new shortcut must be created from the "SIRFFlash.exe" file located at C:\Program Files\SiRF to configure one-click SiRFFlash operation.

Create a new shortcut from the SiRFFlash “SIRFFlash.exe” executable file in the SiRFFlash directory, which by default is installed in the SiRFFlash directory on your C-Drive, located at C:\Program Files\SiRF.

2. Right click on the new shortcut to view the Properties dialog box.



3. Edit the *Target* field under the shortcut tab by adding an input file name and the required argument(s). (See “Using SiRFFlashCL” on page 4-1 for a list of available arguments.)

Argument	Action
-ae	Automatically executes the program
-ax	Automatically exits the program

For example:

```
"C:\Program Files\SiRF\SiRFFlash\SiRFFlash.exe"
GSW3.1_3.1.00.06-C13B1.00.s -ae
```

Loads the file GSW3.1_3.1.00.06-C13B1.00.s and automatically executes the program.

For example:

```
"C:\Program Files\SiRF\SiRFFlash\SiRFFlash.exe"
GSW3.1_3.1.00.06-C13B1.00.s -ae -ax
```

Loads the file GSW3.1_3.1.00.06-C13B1.00.s, automatically executes the program, and automatically exits the program.

4. Click *OK*. Clicking on the new shortcut icon now automatically starts the program and it automatically exits the program when the operation is successfully completed. If not, a window appears and describes the error.

Using SiRFFlash Command Line 4

SiRFFlashCL is capable of two main functions:

- Flash memory programming to one or more GPS receivers
- Reading of flash memory

The following section provides information about how to use the flash memory programming and memory reading functions via SiRFFlashCL, SiRFFlashCL.exe.

Using SiRFFlashCL

SiRFFlashCL is a Windows console application that serves two purposes:

- As the execution vehicle for the SiRFFlash graphical interface program.
- As a standalone command line based application that provides very similar functionality as SiRFFlash, but without using the GUI. It may be used when the GUI is considered unnecessary, such as in batch files.

Before attempting to use the flash memory programming function of SiRFFlashCL, the GPS receiver must be connected to the PC being used, powered, and operating in internal boot mode. (Note: the -xb option places the receiver in external boot mode.) For details on installation and boot mode operation, see “Installing the Hardware” on page 2-2 and “Placing The GPS Receiver in Internal Boot Mode” on page 6-1.

When used as a standalone application, SiRFFlashCL may also be used for programming multiple targets in parallel.

SiRFFlashCL invocation syntax is:

```
SiRFflashcl <filename> [<option>...]
```

The <filename> represents the file to be programmed to flash or the file to be written (when reading flash); options may be:

```
-l N – communication line list / default is -l 1 (i.e. com1)
-b N–baud rate N = 38400, 57600, 115200, 230400, 307200, 460800, 9216 / default is -b 115200
-o N –chip offset / default is -o 0
-c N – chip select N = 0 .. 7 / default is -c 0 (i.e. CSN0)
-e – erase whole chip(s) before programming / default is relevant sectors
```

```
-u   – update sectors / default is erase sectors
-r – read from flash / default is program flash
-f – read from address
-t – read to address
-rw – read whole flash
-jef – just erase flash
-df – detect flash
-q – quiet mode i.e. no info displayed
-sr – save result in RESCOMn
-hd – half duplex communication / default is full duplex
-xb – target is in external boot mode / default is internal
-mrt N – minimal read timeout in millisec / default is 2000
```

SiRFFlashCL is capable of programming multiple targets in parallel. Communication lines used for programming should be specified as a comma separated list, with elements that are either individual port numbers or ranges of numbers, for example 1,3-5 for lines 1, 3, 4, and 5. A list of communication lines cannot contain any spaces. The same input file is programmed to all GPS receivers, and the same controls specified on the SiRFFlashCL invocation line are applied to all GPS receiver connections. The GPS receivers need not contain the same GPS or flash chips.

If successful, SiRFFlashCL returns exit code 0; if it fails, exit code is nonzero. If -sr control is specified, SiRFFlashCL stores text “PASS” in the file(s) RESCOMn (where n represents the port number); if it fails, “FAIL” is stored. File(s) RESCOMn is located in SiRFFlash directory.

Note – To use rates above 115200 Baud, the host computer should be able to support higher Baud rates. The GPS receiver should be equipped with an adequate RS-232 transceiver chip that supports 250Kbps/1Mbps Baud rate. If a USB-to-serial converter is used, a Baud rate of 307200 is typically not supported. For communication via Bluetooth, 38400 Baud should be used.

Note – The <filename> should be enclosed in quotes (“ ”) if it contains any spaces, for example “source file.s”.

Flash Programming Considerations 5

The only file needed when programming flash memory in a SiRF Evaluation Receiver or Development Board is a *.S file (GSW2, SiRFXTrac, or GSW3 for example). However, a binary file (.bin), an Intel hex file (.hex), or an ARM executable file (.axf) may also be used.

Working with Input Files

The SiRFFlash program supports four input file formats:

- Motorola S record (typical extension ".s")
- Intel Hex (typical extension ".hex")
- Binary (typical extension ".bin")
- Arm Executable File (typical extension ".axf")

The SiRFFlash program assumes that address information present (implicitly, such as binary files, or explicitly, such as Motorola S or Intel Hex files) represents offsets from the beginning of the area selected by chip select and chip offset. In those cases, "flash chip view" approach is used.

SiRFFlash interprets the file contents based on content and not based on the file extension. For example, when the first character in the file is 'S', SiRFFlash attempts to interpret the file contents as Motorola S records, if it is a ':', it attempts to interpret Intel Hex records; otherwise it checks if file contains "ELF" signature and if it is an executable; if yes, it is interpreted as an Arm executable in ELF format; otherwise it is considered to be plain Binary.

In an AXF file, the address interpretation is "processor view" based, and data is programmed to flash if the address range specified within the file is within one of the following ranges:

- Starting at chip_select_no * 0x0100 0000 + chip_offset, chip_size long, e.g. for 1 megabyte chip at chip_select_no 0 and chip_offset 0 between 0 and 0x0010 0000
- Starting at 0x4000 0000 + chip_select_no * 0x0100 0000 + chip offset, chip_size long, e.g. for 1 megabyte chip at chip_select_no 0 and chip_offset 0 between 0x4000 0000 and 0x4010 0000

Binary files are the easiest to process and using them as inputs may reduce SiRFFlash execution times.

Communication Settings

Because communication speed most influences the execution time of the SiRFFlash program, the highest possible Baud rate should be used. On most systems, the Baud rate is 115200. However, if the host computer supports higher Baud rates (230400/307200/460800/921600), and the GPS receiver is equipped with adequate RS-232 transceivers (supporting those speeds), higher speeds may be used. Only in rare instances should speeds of 57600 and 38400 be used.

At 115200 Baud, SiRFFlash can program around 12KB of data per second; while at 307200 Baud this increases to as high as 26KB per second. On GSP3 based receivers, set at 921600 Baud, as much as 70KB per second can be programmed.

Full duplex should be selected for maximum transmission rate. This communication method puts the most pressure on the host PC system. When the programming process fails due to a communication problem (typically at the highest Baud rates), using half duplex should be tried. Half duplex communication is only used in internal boot mode.

When programming GPS receivers via a Bluetooth connection, a baud rate of 38400 baud should be used.

GSP3/GSP2 Serial Ports and Baud Rates

SiRFFlash software normally communicates with the host (PC) and the GPS receiver via port A. When only one serial connector is available on your GPS receiver, that is port A. Both GSP3 and GSP2 chips are equipped with two serial ports.

SiRF Equipment	Serial Location
S2SDK and SDKL System Development Boards	Port A serial connector is marked ‘P1’
SiRF Technology Evaluation Kit box	Port A serial connector is marked ‘Com A’

GPS receivers with newer RS-232 transceivers supporting 250Kbps and 1Mbps (such as S3SDK, S2SDK System Development Board, Rev E and higher, or SDKL System Development Board) allow communication at 230400 and 307200 Baud. The S3SDK board is equipped with 1Mbps transceivers, allow communication at 921600 Baud.

Equipment Type	Max. Baud Rate Supported
SiRFstarII Architecture	307200
SiRFstarIII Architecture	921600

External Data Bus Width

SiRFFlash offer a range of external data bus settings. If the external data bus width is selectable on your GSP2 based target, make sure that proper selection is made. GSP3f and GSP2A chips have 16-bit wide external data bus. The SiRF Technology Evaluation Kit box also has a 16-bit wide external data bus. Some GPS receivers offer selectable data bus widths, which are described in Table 5-1

Table 5-1 External Data Bus Width Settings

Equipment	External Data Bus Width
S2SDK System Development Board	16-bit width: Jumper J23 in position 1-2 and jumper J25 in position 2-3. 32-bit width: Jumper J23 in position 2-3 and jumper J25 in position 1-2.
SDKL System Development Board	16-bit width: Jumper J44 in position 1-2, jumper J46 in position 2-3, jumper J68 is in, and jumper blocks J49 and J51 are in. 32-bit width: Jumper J44 in position 2-3, J46 in position 1-2, jumper J67 is in, and jumper blocks J48 and J50 are in.
GPS Receivers with a GSP2e and GSP2e/LP Chip	16-bit width: DATA15 is LOW and DATA7 is HIGH on reset. 32-bit width: DATA15 is HIGH and DATA7 is LOW on reset.

Supporting Different Flash Types

SiRFFlash has the ability to program a wide range of flash memory types. Flash memory types directly supported are listed in the file called `CHIPLIST.TXT`. This file is located in the SiRFFlash installation directory.

Each flash type is described by a line that contains the following information:

- Device name
- Manufacturer name
- Device code (ID)
- Manufacturer code (ID)
- Capacity and sector map
- Driver file name
- Driver parameters

If the flash type that you are using is not listed in the `CHIPLIST.TXT` file, SiRFFlash may still work with that flash type. All you may need to do is add a line to the `CHIPLIST.TXT` file.

To support additional flash types:

1. Obtain the device code (ID), manufacturer code (ID), capacity, and sector map information for the intended flash type. This information is typically available from the flash data sheet.
2. Using a text editor, open the `CHIPLIST.TXT` file.
3. Using the same format that is already in the file, add the device name, manufacturer name, device code, manufacturer code, capacity and sector map information, and the driver file name and parameters at the bottom of the existing list.

   The driver file name must be `GENERIC.BIN`.

SiRFFlash should now be able to be used to program or read the added flash memory type.

Chiplist File Example

This file contains a list of supported devices.

Note – Chips marked with (*) have not been tested by SiRF, but are believed to work with SiRFFlash based on their similarity to other chips on the list.

Device Name	Manuf. Name	Device Code	Manuf. Code	Capacity and Sector Map	Driver File	Options Name	
AM29LV200B	AMD	0x22bf	0x01	0x40000(1*0x4000+2*0x2000+1*0x8000+3*0x10000)	generic.bin		
AM29LV400BB	AMD	0x22ba	0x01	0x80000(1*0x4000+2*0x2000+1*0x8000+7*0x10000)	generic.bin		
AM29LV400BT*	AMD	0x22b9	0x01	0x80000(7*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
AM29DL400BB*	AMD	0x220f	0x01	0x80000(1*0x4000+1*0x8000+4*0x2000+1*0x8000+1*0x4000+6*0x10000)	generic.bin		
AM29DL400BT	AMD	0x220c	0x01	0x80000(6*0x10000+1*0x4000+1*0x8000+4*0x2000+1*0x8000+1*0x4000)	generic.bin		
AM29LV800BB	AMD	0x225b	0x01	0x100000(1*0x4000+2*0x2000+1*0x8000+15*0x10000)	generic.bin		
AM29LV800BT	AMD	0x22da	0x01	0x100000(15*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
AM29DL800BB	AMD	0x22cb	0x01	0x100000(1*0x4000+1*0x8000+4*0x2000+1*0x8000+1*0x4000+14*0x10000)	generic.bin		
AM29DL800BT	AMD	0x224a	0x01	0x100000(14*0x10000+1*0x4000+1*0x8000+4*0x2000+1*0x8000+1*0x4000)	generic.bin		
AM29LV160DB	AMD	0x2249	0x01	0x200000(1*0x4000+2*0x2000+1*0x8000+31*0x10000)	generic.bin		
AM29LV160DT	AMD	0x22c4	0x01	0x200000(31*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
AM29DL161DB*	AMD	0x2239	0x01	0x200000(8*0x2000+31*0x10000)	generic.bin		
AM29DL161DT*	AMD	0x2236	0x01	0x200000(31*0x10000+8*0x2000)	generic.bin		
AM29DL162DB*	AMD	0x222e	0x01	0x200000(8*0x2000+31*0x10000)	generic.bin		
AM29DL162DT	AMD	0x222d	0x01	0x200000(31*0x10000+8*0x2000)	generic.bin		
AM29DL163DB*	AMD	0x222b	0x01	0x200000(8*0x2000+31*0x10000)	generic.bin		
AM29DL163DT	AMD	0x2228	0x01	0x200000(31*0x10000+8*0x2000)	generic.bin		
AM29DL164DB*	AMD	0x2235	0x01	0x200000(8*0x2000+31*0x10000)	generic.bin		
AM29DL164DT	AMD	0x2233	0x01	0x200000(31*0x10000+8*0x2000)	generic.bin		
AM29LV320MB*	AMD	0x227e	0x01	0x400000(8*0x2000+63*0x10000)	generic.bin	DEVCOD2=0x221A	DEVCOD3=0x2200
AM29LV320MT	AMD	0x227e	0x01	0x400000(63*0x10000+8*0x2000)	generic.bin	DEVCOD2=0x221A	DEVCOD3=0x2201
AM29LV640MB	AMD	0x227e	0x01	0x800000(8*0x2000+127*0x10000)	generic.bin	DEVCOD2=0x2210	DEVCOD3=0x2200
AM29LV640MT	AMD	0x227e	0x01	0x800000(127*0x10000+8*0x2000)	generic.bin	DEVCOD2=0x2210	DEVCOD3=0x2201
A29L400UV	AMIC	0xb3b5	0x37	0x80000(1*0x4000+2*0x2000+1*0x8000+7*0x10000)	eneric.bin		
A29L400TV	AMIC	0xb334	0x37	0x80000(7*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
A29L800UV	AMIC	0xb39b	0x37	0x100000(1*0x4000+2*0x2000+1*0x8000+15*0x10000)	generic.bin		
A29L800TV	AMIC	0xb31a	0x37	0x100000(15*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
A29L160UV	AMIC	0xb329	0x37	0x200000(1*0x4000+2*0x2000+1*0x8000+31*0x10000)	generic.bin		
A29L160TV	AMIC	0xb3a8	0x37	0x200000(31*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
AT49BV2048A	ATMEL	0x82	0x1f	0x40000(1*0x4000+2*0x2000+1*0x38000)	generic.bin		
AT49BV4096A	ATMEL	0x1692	0x161f	0x80000(1*0x4000+2*0x2000+1*0x78000)	generic.bin		
AT49BV802A	ATMEL	0xc1	0x1f	0x100000(8*0x2000+15*0x10000)	generic.bin		
AT49BV802AT	ATMEL	0xc3	0x1f	0x100000(15*0x10000+8*0x2000)	generic.bin		
EN29LV400B	EON	0x22ba	0x7f	0x80000(1*0x4000+2*0x2000+1*0x8000+7*0x10000)	generic.bin		
EN29LV400T	EON	0x22b9	0x7f	0x80000(7*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
EN29LV800AB	EON	0x225b	0x7f	0x100000(1*0x4000+2*0x2000+1*0x8000+15*0x10000)	generic.bin		
EN29LV800AT	EON	0x22da	0x7f	0x100000(15*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
EN29SL400B	EON	0x22f1	0x7f	0x80000(1*0x4000+2*0x2000+1*0x8000+7*0x10000)	generic.bin		
EN29SL400T	EON	0x2270	0x7f	0x80000(7*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		
EN29SL800B	EON	0x226b	0x7f	0x100000(1*0x4000+2*0x2000+1*0x8000+15*0x10000)	generic.bin		
EN29SL800T	EON	0x22ea	0x7f	0x100000(15*0x10000+1*0x8000+2*0x2000+1*0x4000)	generic.bin		

```
29LV160BE       FUJITSU   0x2249     0x04     0x200000(1*0x4000+2*0x2000+1*0x8000+31*0x10000)                  generic.bin
29LV160TE       FUJITSU   0x22c4     0x04     0x200000(31*0x10000+1*0x8000+2*0x2000+1*0x4000)                  generic.bin

28F800B3B       INTEL     0x8893     0x89     0x100000(8*0x2000+15*0x10000)                                    generica.bin
28F800B3T       INTEL     0x8892     0x89     0x100000(15*0x10000+8*0x2000)                                    generica.bin
28F800C3B       INTEL     0x88c1     0x89     0x100000(8*0x2000+15*0x10000)                                    generica.bin    SOFT_LOCK_UNLOCK
28F800C3T*      INTEL     0x88c0     0x89     0x100000(15*0x10000+8*0x2000)                                    generica.bin    SOFT_LOCK_UNLOCK
28F160B3B*      INTEL     0x8891     0x89     0x200000(8*0x2000+31*0x10000)                                    generica.bin
28F160B3T*      INTEL     0x8890     0x89     0x200000(31*0x10000+8*0x2000)                                    generica.bin
28F160C3B       INTEL     0x88c3     0x89     0x200000(8*0x2000+31*0x10000)                                    generica.bin    SOFT_LOCK_UNLOCK
28F160C3T*      INTEL     0x88c2     0x89     0x200000(31*0x10000+8*0x2000)                                    generica.bin    SOFT_LOCK_UNLOCK

MX29LV400B      MACRONIX  0x22ba     0xc2     0x80000(1*0x4000+2*0x2000+1*0x8000+7*0x10000)                    generic.bin
MX29LV400T      MACRONIX  0x22b9     0xc2     0x80000(7*0x10000+1*0x8000+2*0x2000+1*0x4000)                    generic.bin
MX29LV800BB     MACRONIX  0x225b     0xc2     0x100000(1*0x4000+2*0x2000+1*0x8000+15*0x10000)                  generic.bin
MX29LV800BT     MACRONIX  0x22da     0xc2     0x100000(15*0x10000+1*0x8000+2*0x2000+1*0x4000)                  generic.bin
MX29LV160BB     MACRONIX  0x2249     0xc2     0x200000(1*0x4000+2*0x2000+1*0x8000+31*0x10000)                  generic.bin
MX29LV160BT     MACRONIX  0x22c4     0xc2     0x200000(31*0x10000+1*0x8000+2*0x2000+1*0x4000)                  generic.bin
MX69LW1641B*    MACRONIX  0xa1       0x1c     0x200000(8*0x8000+28*0x10000)                                    generica.bin    SOFT_LOCK_UNLOCK
USE_PAGE256_WRITE
MX69LW1641T     MACRONIX  0xa0       0x1c     0x200000(28*0x10000+8*0x8000)                                    generica.bin    SOFT_LOCK_UNLOCK
USE_PAGE256_WRITE
MX69LW3241B*    MACRONIX  0x21       0x1c     0x400000(8*0x2000+63*0x10000)                                    generica.bin    SOFT_LOCK_UNLOCK
USE_PAGE256_WRITE
MX69LW3241T*    MACRONIX  0x20       0x1c     0x400000(63*0x10000+8*0x2000)                                    generica.bin    SOFT_LOCK_UNLOCK
USE_PAGE256_WRITE

LE28FV4101T     SANYO     0x2        0x62     0x80000(256*0x800)                                               generic.bin     NO_ERROR_BITS
LE28FW8203T     SANYO     0x2d       0x62     0x100000(15*0x10000+1*0x8000+2*0x2000+1*0x4000)                  generic.bin

LH28F800BVE     SHARP     0x4b       0xb0     0x100000(8*0x2000+15*0x10000)                                    generica.bin
LH28F800BJHE    SHARP     0xed       0xb0     0x100000(8*0x2000+15*0x10000)                                    generica.bin    SOFT_LOCK_UNLOCK
LH28F800BJE     SHARP     0xec       0xb0     0x100000(15*0x10000+8*0x2000)                                    generica.bin    SOFT_LOCK_UNLOCK
LH28F160BJHE    SHARP     0xe9       0xb0     0x200000(8*0x2000+31*0x10000)                                    generica.bin    SOFT_LOCK_UNLOCK

SST39VF400A     SST       0x2780     0xbf     0x80000(128*0x1000)                                              generic.bin     NO_ERROR_BITS

SST39WF400A     SST       0x272f     0xbf     0x80000(128*0x1000)                                              generic.bin     NO_ERROR_BITS
SST39VF800      SST       0x2781     0xbf     0x100000(256*0x1000)                                             generic.bin     NO_ERROR_BITS
SST39WF800A     SST       0x273f     0xbf     0x100000(256*0x1000)                                             generic.bin     NO_ERROR_BITS
SST39VF160      SST       0x2782     0xbf     0x200000(512*0x1000)                                             generic.bin     NO_ERROR_BITS
SST39VF1601     SST       0x234b     0xbf     0x200000(512*0x1000)                                             generic.bin     NO_ERROR_BITS
SST39VF1602*    SST       0x234a     0xbf     0x200000(512*0x1000)                                             generic.bin     NO_ERROR_BITS

M29W400BB       ST        0xef       0x20     0x80000(1*0x4000+2*0x2000+1*0x8000+7*0x10000)                    generic.bin
M29W400BT       ST        0xee       0x20     0x80000(7*0x10000+1*0x8000+2*0x2000+1*0x4000)                    generic.bin
M29W800AB       ST        0x5b       0x20     0x100000(1*0x4000+2*0x2000+1*0x8000+15*0x10000)                  generic.bin
M29W800AT       ST        0xd7       0x20     0x100000(15*0x10000+1*0x8000+2*0x2000+1*0x4000)                  generic.bin
M29W800DB       ST        0x225b     0x20     0x100000(1*0x4000+2*0x2000+1*0x8000+15*0x10000)                  generic.bin
M29W800DT       ST        0x22d7     0x20     0x100000(15*0x10000+1*0x8000+2*0x2000+1*0x4000)                  generic.bin
M29W160EB       ST        0x2249     0x20     0x200000(1*0x4000+2*0x2000+1*0x8000+31*0x10000)                  generic.bin
M29W160ET       ST        0x22c4     0x20     0x200000(31*0x10000+1*0x8000+2*0x2000+1*0x4000)                  generic.bin
M28W800CB       ST        0x88cd     0x20     0x100000(8*0x2000+15*0x10000)                                    generica.bin    SOFT_LOCK_UNLOCK
M28W800CT       ST        0x88cc     0x20     0x100000(15*0x10000+8*0x2000)                                    generica.bin    SOFT_LOCK_UNLOCK

TC58FVB400      TOSHIBA   0x4c       0x98     0x80000(1*0x4000+2*0x2000+1*0x8000+7*0x10000)                    generic.bin
TC58FVB160AFT   TOSHIBA   0x43       0x98     0x200000(1*0x4000+2*0x2000+1*0x8000+31*0x10000)                  generic.bin
TC58FVT160AFT   TOSHIBA   0xc2       0x98     0x200000(31*0x10000+1*0x8000+2*0x2000+1*0x4000)                  generic.bin
```

Note – Chiplist file last updated July 24, 2006

Receiver Boot Mode 6

When a GPS receiver is powered on, it reads several flags, one of which determines whether the device is in internal or external boot mode. See “How Boot Mode is Determined at Power On” on page 6-4 for a detailed explanation. The following sections explain how to change the boot mode on a SiRF GPS receiver.

Placing The GPS Receiver in Internal Boot Mode

Before any flash memory in a SiRF Evaluation Receiver or Development Board can be programmed or read, it is necessary to place the GPS receiver in internal boot mode.

To place an Evaluation Receiver or Development Board in internal boot mode:

1. Locate the required boot switch and place it in internal boot mode position.

   This is different for each SiRF GPS receiver. Table 6-1 provides information on the location and setting of the boot switch for SiRF GPS receivers.

2. Power cycle the GPS receiver (off, then on) or press the Restart switch.

   The GPS receiver is now in internal boot mode.

3. SiRFFlash can now be used to either program or read flash memory.

4. After programming or reading of the flash memory, return the GPS receiver to external boot mode.

   See Table 6-1 for information on the location and setting of the boot switch to return different SiRF GPS receivers to external boot mode.

Note – Placing a switch in a position does NOT place the GPS receiver in the corresponding mode; it only sets the flags. The receiver enters the designated mode when a subsequent reset or power cycle occurs.

Table 6-1 SiRF Receivers and Boot Switch Settings

Receiver	Boot Switch Information
GSD3tw Evaluation Receiver	Located on the front panel, the boot switch is labeled *Flash* and has two positions. Depending on the receiver, these two positions will be: *Run* and *Flash*. For all receivers, when this switch is in the *Flash* position, the GPS receiver can be placed in internal boot mode by cycling power. To return to external boot mode, place the switch in the *Run* position and again cycle power.
SiRFstarIII (GSC3f/LPx, GSC3f/LP, GSC3f/LPa, GSC3LTf/LTif) Evaluation Receiver	Located on the front panel, the boot switch is labeled *Flash* and has three positions. Depending on the receiver, these three positions will be: *Run*, *Flash*, and *NU* or *Run ROM*, *Flash*, and *Run Flash*. For all receivers, when this switch is in the *Flash* position (center), the GPS receiver can be placed in internal boot mode by cycling power. To return to external boot mode, place the switch in the *Run* (or *Run Flash*) position and again cycle power.
GSC3LTf/LTif SiRFLoc Client Evaluation Receiver	GSC3LTf/LTif SiRFLoc Receiver: Located on the front panel, the boot switch has three positions: *Run*, *Flash*, and *NU*. When this switch is in the *Flash* position the Receiver is in internal boot mode. This switch must be returned to the *Run* position for normal operation in external boot mode. The Receiver may also be flashed via the ANE by positioning the ANE's switch to *SLC* and positioning the Receiver switch to *Flash*. SiRFLoc Aided GPS Network Emulator (ANE): Located on the front panel, the boot switch is labeled TTB has two positions: *Boot* and *Run*. When this switch is in the *Boot* position, the ANE is in internal boot mode. This switch must be returned to the *Run* position for normal operation in external boot mode.
GSC3f SiRFLoc Client Evaluation Receiver	GSC3f SiRFLoc Receiver: Located on the front panel, the boot switch has three positions: *Run*, *Flash*, and *NU*. When this switch is in the *Flash* position the Receiver is in internal boot mode. This switch must be returned to the *Run* position for normal operation in external boot mode. The Receiver may also be flashed via the ANE by positioning the ANE's switch to *SLC* and positioning the Receiver switch to *Flash*. SiRFLoc Aided GPS Network Emulator (ANE): Located on the front panel, the boot switch is labeled TTB has two positions: *Boot* and *Run*. When this switch is in the *Boot* position, the ANE is in internal boot mode. This switch must be returned to the *Run* position for normal operation in external boot mode.
SiRFDiRect Evaluation Receiver	Located on the front panel, the boot switch is labeled *Flash* and has three positions: *Run ROM*, *Flash*, and *Run Flash*. When this switch is in the *Flash* position (center), the GPS receiver can be placed in internal boot mode by cycling power. To return to external boot mode, place the switch in the *Run Flash* position and again cycle power.
SiRFstarIIe/LP Evaluation Receiver	Located on the front panel, the boot switch is labeled either *Xtrac*, *Boot*, and *GSW2*, or *Boot* and *Data*, depending on the model of GPS receiver you have. When this switch is in the *Boot* position and the *Reset* switch (labeled *Fn*) is pressed, or power is cycled, the GPS receiver enters internal boot mode. To return to external boot mode, return the switch to the appropriate position for the software you have loaded and either cycle power or again press the *Reset* switch.
SiRFLoc 2.0 Evaluation Receiver	Located on the front panel, the boot switch is labeled *Boot Mode* and has three positions: *TTB*, *NORMAL*, and *SLC*. If placed in the *TTB* position, internal Time Transfer Board is placed in internal boot mode. If placed in the *SLC* position, internal SiRFLoc Client board is placed in external boot mode. The *Boot Mode* switch must be returned to *NORMAL* for normal operation in external boot mode.
SiRFDRive Evaluation Receiver	Located on the front panel, the boot switch has three positions: *Not Used*, *Boot*, and *SiRFDRive / GSW2*. If placed in the *Boot* position and the receiver's power is cycled, the GPS receiver is placed in internal boot mode. The switch must be returned to the *SiRFDRive / GSW2* position for normal operation in external boot mode.
GSP2 Evaluation Receiver	The processor boots in internal mode when the switch *BOOT/DATA* is in the *BOOT* position. It is in external boot mode when the switch is in the *DATA* position.
SiRFstarIII (GSC3f/LPx, GSC3f/LP) Development Board	Located on the front panel, the boot switch is labeled *FLASH* and has three positions: *3E*, *FLASH*, and *NU*. When this switch is in the *FLASH* position the GPS receiver is in internal boot mode. This switch must be returned to the *3E* position for normal operation in external boot mode.

Table 6-1 SiRF Receivers and Boot Switch Settings *(Continued)*

S2SDK Development Board	The processor boots in internal boot mode when jumper J21 is in position 1-2. It boots in external boot mode when J21 is in position2-3.
SDKL Development Board	The boot switch is a toggle switch located on the side of the board labeled S3 and has two positions: *INT* and *EXT*. The board is in internal boot mode when the switch is in the *INT* position. This switch must be returned to *EXT* for normal operation in external boot mode.
SDKL-DR Development Board	The boot switch is a toggle switch located on the side of the board labeled S3 and has two positions: *INT* and *EXT*. The board is in internal boot mode when the switch is in the *INT* position. This switch must be returned to *EXT* for normal operation in external boot mode.

External Boot Mode

A GPS receiver operating in external boot mode typically executes—and generally supports—both the NMEA and SiRF binary protocols. Most GPS receivers can be placed in internal boot mode using a SiRF binary command. If the GPS receiver is operating in NMEA protocol, first transfer to SiRF binary protocol using the appropriate command.

In SiRF binary protocol, Message ID 148, Flash Update message, must be supported by the software. Refer to your documentation and the table below to determine if your GPS receiver and software supports both SiRF binary protocol and Message ID 148.

In external boot mode, a GSP3 or GSP2 baseband chip typically executes SiRF Technology's GSW™, SiRFLoc™, or SiRFXTrac® software, in which case, reprogramming of flash chip is possible in the following cases:

Table 6-2

Output	Protocol	Action
GSP3/GSP2 chip output	NMEA	Set Serial Port message ($PSRF 100), which initiates switching to SiRF binary protocol, should be supported; in addition to that, SiRF binary protocol and Flash Update message (ID 148) within that protocol should be supported
GSP3/GSP2 chip output	SiRF Binary	Flash Update message (ID 148) should be supported
GSP3/GSP2 chip output	SiRFLoc Binary	Flash Update message (ID 148) should be supported

The ability to reprogram the flash in external boot mode is critically dependent on the ability of the code already present in flash to recognize the commands in the table above.

Use internal boot mode for flashing whenever a selection between internal and external boot mode is available. If flash programming in external boot mode is the only option, make sure that target device power is available during whole programming process.

Note – The GPS receiver must be fully powered during the programming process, especially when the device is battery operated.

If the reprogramming process fails, reset the GPS receiver, and retry the operation.

How Boot Mode is Determined at Power On

When a GPS receiver is powered on or when it executes a hard reset (reset switch activated), it reads some flags created by pull-up and pull-down resistors placed on various bus lines. The flag on data bus 0 determines the boot mode. If data bus bit 0 has a pull-down resistor on it, the GPS receiver enters external boot mode. This is the normal operating mode of the GPS receiver, when the computer instructions are coming from the normal program location. If the data bus line has a pull-up resistor on it, the GPS receiver enters internal boot mode when instructions come from an internal ROM memory. This ROM contains the software needed to enable flash programming of the GPS receiver. SiRFFlash requires the GPS receiver to be placed in internal boot mode in order to function.

In addition to using the pull-up resistor to enter internal boot mode, some GPS receivers allow use of a binary command (while in external boot mode) to switch to internal boot mode. See the documentation supplied with your GPS receiver to determine if it supports this command.

SiRF receivers operate in two operating modes: internal boot mode and external boot mode. These names are derived from the traditional location of the memory supplying computer instructions:

- Internal boot mode
  Instructions come from the boot ROM, located inside the baseband chip.
- External boot mode
  Instructions come from a flash memory chip external to the baseband chip.

Newer SiRF chipsets include features such as internally mounted flash memory, or internal program ROM. These chipsets still include the internal boot ROM, and internal boot mode still implies executing the code from that boot ROM. External boot mode always means executing from the memory where the normal GPS software resides, regardless of where the program memory is physically located.

Troubleshooting A

The following error messages are generated by SiRFFlash when programming errors occur. Descriptions are provided here to help the user correct the programming errors. If the errors persist, contact SiRF Technology.

Error Messages

Table 6-3 Troubleshooting Messages and Descriptions

Error Message	Description
Invocation Line Errors All errors in this group are fatal and cause termination of the SiRFFlash program.	
Error in invocation line	Quotes are used on the invocation line, but they do not match.
Line is not recognized	String following -l option should represent a number.
Specified line does not exist	Line specified on the SiRFFlash command line was not found in the Windows registry section describing COM ports available on your PC.
Speed is not recognized	String following -b option should be one of these numbers: 38400, 57600, 115200, 230400, 307200, 460800, or 921600.
Chip offset is not recognized	String following -o option should be a number.
Chip select is not recognized	String following -c option should be a number between 0 (zero) and 7.
Suspicious chip offset value	User specified chip offset should be a number divisible by 0x20000 (128k).
From address is not recognized	String following -f option should be a number.
To address is not recognized	String following -t option should be a number.
End address lower than start address	Value specified in “From address” field is higher than the value specified in the “To address” field.
Minimal read timeout is not recognized	Argument following -mrt option should be a number.
Option is not recognized	Option (string starting with “-” character) is not recognized. See “Using SiRFFlashCL” on page 4-1, for allowed character options.

Table 6-3 Troubleshooting Messages and Descriptions *(Continued)*

Error Message	Description
Multiple files specified	Multiple strings not starting with "-" character, and interpreted as file names, were found on the SiRFFlash command line. This typically happens when full input or output file name contains spaces, and is not quoted.
Cannot open chiplist file	The SiRFFlash installation directory should contain the file chiplist.txt. That plain text file contains descriptions of all chips supported by SiRFFlash.
Error while processing chiplist file	Syntax error was encountered while processing file chiplist.txt located in the SiRFFlash installation directory.
Cannot open input file	Flash programming operation was selected and the specified file does not exist. Correct the file name by retyping it or by using the *Browse* button.
Cannot create output file	Flash reading operation was selected and the file specified could not be created. Correct the file name by retyping it or by using the *Browse* button.
Write to output file failed	During storing of data read from flash, an error was reported, usually due to lack of disk space.
Cannot open port COMx	Selected port is being used by another application.
Unpopulated area found at specified chip select	No chip(s) have been detected on the specified flash location. Correct the Flash location description.
Data file not specified	Specify the input file (if flash programming is selected) or the output file (if flash reading is selected) by typing its name in the *File selection* field or by using the *Browse* button.
Failed to launch SiRFFlashcl	SiRFFlash was unable to launch SiRFFlashcl.exe—the command line version of SiRFFlash, which performs flash programming/reading. Make sure that the directory in which SiRFFlash.exe is installed contains the file SiRFFlashcl.exe.
Cannot communicate with SiRFFlashcl	SiRFFlash was unable to create pipes to communicate with SiRFFlashcl.exe—the command line version of SiRFFlash, which performs flash programming/reading.
Flash read failed	An error has been reported during flash reading. Retry the operation.
Flash Programming Errors During flash programming a number of error messages may be reported; they reflect problems encountered during the programming process. Retry the procedure. If the problem persists, try half duplex or lower the Baud rate. If that does not resolve the problem, contact SiRF Technology.	
Incompatible chips found	The GPS receiver is configured for a 32-bit external bus and chips found are different. This configuration is not currently supported by SiRFFlash. See "Supporting Different Flash Types" on page 5-3.
Invalid chip offset	Verify that the chip offset field: • Is not blank • Contains correct hex or decimal number • Specifies the address that is on the 1 megabit (128 kilobyte) boundary

Table 6-3 Troubleshooting Messages and Descriptions *(Continued)*

Error Message	Description
Invalid end address	Verify that the To address field contains the correct hex or decimal number specifying the offset within the chip(s) address range and that this value is greater or equal to the value specified in the From address field.
Invalid start address	Verify that the From address field contains the correct hex or decimal number specifying the offset within the chip(s) address range.
RAM found at specified chip select/offset	Memory behaving as RAM was detected at the specified flash location. Correct the Flash location description.
Unknown flash found	A chip that is not on the list of supported chips (file chiplist.txt) has been detected. Follow the procedure for supporting new chips. See “Supporting Different Flash Types” on page 5-3.
Target is not in specified boot mode	Current boot mode detected on the GPS receiver does not match the one selected in the *Target boot mode* setting.
Unknown baseband chip found on the target	Baseband chip found on the GPS receiver is not supported by this version of SiRFFlash.
Unsupported combination of baseband and RF chip found on the target	This version of SiRFFlash does not support the RF chip detected on the GPS receiver. Check for newer version of SiRFFlash at www.sirf.com.
Flash detection software download failed	Software for detecting target platform characteristics (baseband, RF, flash) failed to respond after it was sent to the GPS receiver. Typically, this happens when the PC host and the GPS receiver are not properly connected.
Target communication failure	General communication error. Check connection state and restart the operation.
External bus width found is not 16 or 32	SiRFFlash supports targets with 16- and 32-bit wide data busses only. Retry, and if problem persists check GPS receiver hardware settings.
Failed to get flash chip ids	Operation failed to obtain information identifying flash chips on the GPS receiver in a unique manner. Retry the operation.
Flash driver download failed	Once GPS receiver configuration is detected, SiRFFlash sends a driver program that knows how to program the detected flash, to the GPS receiver. Download process failed. Retry the operation.
Invalid flash driver name	Entry in chiplist.txt file that describes flash chip found on the GPS receiver does not indicate that generic.bin or generica.bin is the name of the flash driver. Correct chipfile using text editor program and retry.
Error reading input file	Defective input file was detected by SiRFFlash. Check that the correct input file was specified, and, if yes, check its contents. Replace file if necessary.
AXF data area not within low or high chip range	Data in AXF input file is beyond chip address range (low and high). Recreate AXF file, and retry. See “Working with Input Files” on page 5-1 for more information.
Highest data address above chip highest address	Part of the data specified in the input file cannot be programmed to flash because its address is higher than chip highest address. Check the input file and retry.

Serial Peripheral Interface Support B

Version 3.40 of SiRFflash supports programming GSC3LT/GSC3LTi targets via Aardvark and Cheetah Serial Peripheral Interface (SPI) adapters from TotalPhase.

LT/LTi targets may be programmed via SPI in internal boot mode only.

For programming via SPI, bit rates are fixed and initially are 3 Mb/sec.

For data transfer:

- Cheetah adapter bit rates are fixed to 1110 kB/sec
- Aardvark adapter bit rates are fixed toto 8 Mb/sec

Note – Aardvark hardware has interbyte interval of 9 µs.

Specifying standard serial bit rate (such as 460800 baud) has no effect on SPI programming.

Due to better performance, full duplex is always used with SPI since it reduces number of idle bytes sent to the target. If half-duplex is specified by the user, request is silently ignored.

Multiple Cheetah and Aardvark adapters may be used at the same time. In SIRFflash, Aardvark adapters are referenced as AARDVARK1, AARDVARK2, and so on. Cheetah adapters are references as CHEETAH1.1, CHEETAH1.2, CHEETAH1.3, CHEETAH2.1, CHEETAH2.2, and so on..

In SiRFflashcl Aardvark adapters are referenced as lines 101, 102 and so on. Cheetah adapters are referenced as lines 211, 212, 213, 221, 222, and so on.

Note – In order to program flash via SPI, USB drivers from TotalPhase should be installed, and DLL files aardvark.dll and/or cheetah.dll should be placed into the SiRFFlash installation directory.

For best performance, SiRF recommends using the Cheetah adapter. Flash programming time with the Cheetah adapter is at least 10 percent faster than serial programming at 921600 baud.

Acronyms and Abbreviations Glossary

C

2-D	Two dimensional
3-D	Three dimensional
A/D	Analog to Digital
AGC	Automatic Gain Control
Almanac	A set of orbital parameters that allows calculation of the approximate GPS satellite positions and velocities. A GPS receiver uses the almanac as an aid to determine satellite visibility during acquisition of GPS satellite signals. The almanac is a subset of satellite ephemeris data and is updated weekly by GPS Control. The almanacs for all 32 possible satellite PRN numbers are sent by the satellites in subframes 4 and 5 of the navigation message, with one satellite almanac in a single subframe. It takes 12.5 minutes for all satellite almanacs to be transmitted.
Altitude	The vertical distance between a reference point and the receiver. In GPS systems, the altitude is always computed with respect to the WGS-84 reference ellipsoid (q.v.). However, the receiver may contain a model that allows it to estimate the mean sea level (MSL) relationship to the reference ellipsoid, and then report MSL altitude as well.
Altitude Hold	A technique that allows navigation using measurements from three GPS satellites plus an independently obtained value of altitude. This permits computing a position solution with less than the normally required 4 satellites.
Altitude Hold Mode	A navigation mode during which a value of altitude is processed by the Kalman Filter as if it were a range measurement from a satellite at the Earth's center (WGS-84 reference ellipsoid center).
BA	Bus Address
BGA	Ball Grid Array
Baud	The rate of change on a serial data line. Often, but not always the same as bits per second (See bps.)
BOM	Bill Of Materials
bps	Bits per second; the rate of data transmission on a serial data bus. In most cases this can be referred to as baud.
C	Celsius, a unit of temperature
C/A Code	Coarse/Acquisition Code. A spread-spectrum, direct-sequence code applied to the GPS satellite carrier signal. This code is typically the only one used by commercial GPS receivers to compute the range between receiver and the satellite. Military receivers use this code only to acquire the satellite signal, and then typically switch to the P code for more precise ranging.

CEP	Circular Error Probable. The radius of a circle, centered at the user's true location, that contains 50 percent of the individual horizontal position measurements made using a particular navigation system.
Clock Error	The uncompensated difference between synchronous GPS system time and time best known within the GPS receiver. Also called Clock Error.
CMOS	Complimentary Metal Oxide Semiconductor
C/N_0	Carrier-to-Noise density ratio. In spread-spectrum systems like GPS, this is equivalent to signal-to-noise ratio in a conventional radio system.
Cold Start	A startup condition in a GPS receiver in which the receiver does not have position, time, or both, and in which it does not have ephemeris. In this type of a start, it must search for satellites without knowing which ones may be visible, and once it finds satellites it must learn their ephemeris by listening to the navigation message of each satellite.
Control Segment	The Master Control Station and the globally dispersed Monitor Stations used to manage the GPS satellites, determine their precise orbital parameters, and synchronize their clocks.
dB	Decibel, a unit of comparative measurement equal to $10\log_{10}$(measurement / reference)
dBiC	Decibel-Isometric-Circular (measure of power relative to an isometric antenna with circular polarization).
dBm	Decibels relative to 1 milliWatt.
dBW	Decibels relative to 1 Watt
DC	Direct Current
DGPS	Differential GPS. A technique to improve GPS accuracy that uses pseudorange errors recorded at known locations to improve the measurements made by other GPS receivers.
Doppler Aiding	A signal processing strategy that uses a measured Doppler shift to help a receiver smoothly track a GPS signal to allow a more precise velocity and position measurement.
DoD	The U.S. Government Department of Defense
DOP	Dilution of Precision (see GDOP, HDOP, PDOP, TDOP, and VDOP).
DRAM	Dynamic Random Access Memory, a form of RAM that maintains its contents as long as power is applied and periodic refresh reads are made. If either power is lost of the refresh signal is not maintained, the contents of the memory will become corrupted.
DSP	Digital Signal Processor
DTR	Data Terminal Ready. A hardware signal that is part of a serial data bus.
ECEF	Earth-Centered Earth-Fixed. A Cartesian coordinate system with its origin located at the mass center of the Earth and whose axes rotate with the Earth. The coordinate system used by GPS to describe 3-D location. For the WGS-84 reference ellipsoid, ECEF coordinates have the Z-axis aligned with the Earth's spin axis, the X-axis through the intersection of the Prime Meridian and the equator, and the Y-axis is rotated 90 degrees East of the X-axis.
EA	External Address
EEPROM	Electrically Erasable Programmable Read Only Memory
EHPE	Estimated Horizontal Position Error
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPE	Estimated Position Error

Ephemeris	A set of satellite orbital parameters used by a GPS receiver to calculate precise GPS satellite positions and velocities. The ephemeris of a satellite is broadcast by that satellite in subframes 1, 2 and 3 of the navigation message. It takes 18 seconds to transmit, and is repeated every 30 seconds.
EPROM	Erasable Programmable Read Only Memory
ESD	Electrostatic Discharge
EVPE	Estimated Vertical Position Error
FP	Floating-Point mathematics, as opposed to integer.
FRP	Federal Radionavigation Plan. The U.S. Government document that contains the official policy on the commercial use of GPS.
FSM	Finite State Machine
GaAs	Gallium Arsenide, a semiconductor material.
GDOP	Geometric Dilution of Precision. A factor used to describe the effect of the satellite geometry on the position and time accuracy of the GPS receiver solution. The lower the value of the GDOP parameter, the less the errors in the position solution. Related indicators include PDOP, HDOP, TDOP, and VDOP.
GMT	Greenwich Mean Time, now commonly called Universal Coordinated Time, or UTC
GPS	The Navstar Global Positioning System. A space-based radio positioning system that provides suitably equipped users with accurate position, velocity, and time data. GPS provides this data free of direct user charge worldwide, continuously, and under all weather conditions. The GPS constellation consists of 24 or more orbiting satellites spaced around each of six different orbital planes. The system is developed by the DoD under Air Force management.
GPS Time	The number of seconds since Saturday/Sunday Midnight, with time zero being this midnight. Used with GPS Week Number to determine a specific point in GPS time. GPS time is related to UTC but differs from it by an integer number of leap seconds, and by a variable time that is normally controlled to be less than 20 ns.
GUI	Graphic User Interface
HDOP	Horizontal Dilution of Precision. A measure of how much the geometry of the satellites affect the position estimate (computed from the satellite range measurements) in the horizontal (East, North) plane.
Held Altitude	The altitude value that is sent to the Kalman filter as a measurement when in Altitude Hold Mode.
Hot Start	A startup mode for a GPS receiver in which the receiver knows the approximate time, its approximate position, and in which it has sufficient ephemerides in its memory so that once it acquires the satellite signals it can compute a solution without having to learn the ephemeris from the satellite navigation messages. The knowledge of approximate time and position permits the receiver to search for those satellites that are known to be visible from the receiver's position.
Hz	Hertz, a unit of frequency (cycles per second).
I/O	Input/Output
IF	Intermediate Frequency
IRQ	Interrupt ReQuest line
ISR	Interrupt Service Routine
IGRF	International Geomagnetic Reference Field
IODC	Issue Of Data Clock, a reference value in the navigation message that indicates the version of clock corrections.

IODE	Issue Of Data Ephemeris, a reference value in the navigation message that indicates the version of orbital parameters. IODE is a subset of IODC.
JPO	Joint Program Office. An office within the U.S. Air Force Systems Command, Space Systems Division. The JPO is responsible of managing the development and production aspect of the GPS system and is staffed by representatives from each branch of the U.S. military, the U.S. Department of Transportation, U.S. Defense Mapping Agency, NATO member nations, and Australia.
Kalman Filter	Sequential estimation filter that combines measurements of satellite range and range rate with the last-computed position to determine the position, velocity, and time at the GPS receiver antenna.
km	Kilometer (1 km = 1000 meters).
L1	The 1575.42MHz GPS carrier frequency that contains the C/A code, P-code, and navigation messages used by commercial GPS receivers.
L2	A secondary GPS carrier, containing only P-code, used primarily to calculate signal delays caused by the atmosphere. The L2 frequency is 1227.60MHz.
Latitude	Halfway between the poles lies the equator. Latitude is the angular measurement of a place expressed in degrees north or south of the equator. Latitude runs from 0° at the equator to 90°N or 90°S at the poles. When not qualified with letters N or S, it is assumed positive is north of the equator and negative is south of the equator. Lines of latitude run in an east-west direction. They are called parallels.
LLA	Latitude, Longitude, Altitude. Geographical coordinate system used for locating places on the surface of the Earth. Latitude and longitude are angular measurements, expressed as degrees of a circle measured from the center of the Earth. The Earth spins on its axis, which intersects the surface at the north and south poles. The poles are the natural starting place for the graticule, a spherical grid of latitude and longitude lines. See also Altitude.
LNA	Low Noise Amplifier
Longitude	Lines of longitude, called meridians, run in a north-south direction from pole to pole. Longitude is the angular measurement of a place east or west of the prime meridian. This meridian is also known as the Greenwich Meridian, because it runs through the original site of the Royal Observatory, which was located at Greenwich, just outside London, England. Longitude runs from 0° at the prime meridian to 180° east or west, halfway around the globe. When not qualified with letters E or W, it is assumed positive is east of Greenwich and negative is west of Greenwich. The International Date Line follows the 180° meridian, making a few jogs to avoid cutting through land areas.
LPTS	Low Power Time Source
LSB	Least Significant Bit or Bytes of a binary word
LTP	Local Tangent Plane coordinate system. The coordinates are supplied in a North, East, Down sense. The North and East are in degrees or radians, and Down is height below WGS-84 ellipsoid in meters.
m/s	Meters per second (unit of velocity)
m/s/s or m/s^2	Meters per second per second (unit of acceleration)
m/s/s/s or m/s^3	Meters per second per second per second (unit of impulse or “jerk”)
Mask Angle	An angle of elevation (angle above the local horizontal) which is the limit for using satellites in a navigation solution. Because low-elevation satellites tend to have more multipath problems, GPS receivers set a mask angle and will not use satellites whose elevation is below that angle. Typical mask angles are 5º, 10º and 15º.
MID	Message Identifier. In the case of SiRF binary protocol, it is a number between 1 and 255.

MIPS	Million Instructions Per Second, a measurement of the speed of a computer
MHz	Megahertz, a unit of frequency equal to one million Hz
MSB	Most Significant Bit within a binary word
MSL	Mean Sea Level
MTBF	Mean Time Between Failures
MUL	Memory Upper Lower, a control line on SiRF baseband chips used to select part of a memory word.
Multipath Error	GPS positioning errors caused by the interaction of the GPS satellite signal and its reflections.
mV	Millivolt
mW	Milliwatt
NED	North, East, Down coordinate system. See LTP.
Navigation Message	The data added to the GPS satellites' PRN codes. The navigation message is composed of data bits sent at 50 bps. Data words consist of 30 consecutive bits, and contain 24 bits of actual data and 6 bits or error detection codes. A group of 10 consecutive words are called a subframe. 5 consecutive subframes are called a frame. 25 consecutive frames are called a super frame. The 5 subframes that form a frame contain the transmitting satellite's ephemeris and clock correction in the first 3 subframes, and system information such as satellite almanacs in the remaining 2 subframes.
NF	Noise Factor
NMEA	National Marine Electronic Association. Also commonly used to refer to NMEA 0183, Standard for Interfacing Marine Electronic Devices, a serial message protocol commonly used by GPS receivers.
NVRAM	Non-volatile Random Access Memory, portion of the SRAM that is powered by a backup battery power supply when prime power is removed. It is used to preserve important data and allow faster entry into the Navigation Mode when prime power is restored.
Obscuration	Term used to describe periods of time during which a GPS receiver's line-of-sight to GPS satellites is blocked by natural or man-made objects.
OEM	Original Equipment Manufacturer
Overdetermined Solution	The solution of a system of equations containing more equations than unknowns. The GPS receiver computes, when possible, an overdetermined solution using the measurements from five or more GPS satellites, instead of the four necessary for a three-dimensional position solution.
P-Code	Precise Code. A spread spectrum direct sequence code that is used primarily by military GPS receivers to determine the range to the transmitting GPS satellite.
Parallel Receiver	A receiver that monitors four or more satellites simultaneously. SiRF receivers can monitor 12 or more satellites simultaneously.
PDOP	Position Dilution of Precision. A measure of how much the error in the three-dimensional position estimate produced from satellite range measurements is amplified by a poor satellite geometry with respect to the receiver antenna.
Pi	The mathematical constant having a value of approximately 3.14159
P-P	Peak to Peak
PPS	Precise Positioning Service. The GPS positioning, velocity, and time services that are available on a continuous, worldwide basis to users authorized by the DoD.

PRN	PseudoRandom Number. The identity of the GPS satellites as determined by a GPS receiver. Since all GPS satellites must transmit on the same frequency, they are distinguished by their pseudorandom number codes, which range from 1 to 32.
Pseudorange	The calculated range from the GPS receiver to the satellite, which is determined by measuring the phrase shift of the PRN code received from the satellite with internally generated PRN code from the receiver. Because of atmospheric and timing effects, this time is not exact. Therefore, it is called a pseudorange instead of a true range.
PVT	Position, Velocity, and Time
RAM	Random Access Memory, a form of computer memory that may be read and written to by the processor.
Receiver Channels	A GPS receiver specification that indicates the number of independent hardware signal processing channels or unique tracking resources included in the receiver design.
RF	Radio Frequency
RFI	Radio Frequency Interference
ROM	Read Only Memory, a form of computer memory that may be read by the processor, but not written to.
RTC	real-time Clock
RTCA	A private, not-for-profit corporation that develops consensus-based recommendations regarding communications, navigation, surveillance, and air traffic management (CNS/ATM) system issues. Previously called Radio Technical Commission for Aeronautics
RTCM	The Radio Technical Commission for Maritime Services, an organization that sets standards for marine communications. Special Committee 104 of the RTCM established and maintains a communications protocol that is used in GPS receivers to send DGPS corrections between reference receivers and receivers using the corrections.
SA	Selective Availability. The method used by the DoD to control access to the full accuracy achievable with the C/A code. In May, 2000, the DoD elected to turn SA off, and may not use it again.
Satellite Elevation	The angle of the satellite above the horizon
SEP	Spherical Error Probable. The radius of a sphere, centered at the user's true location, that contains 50 percent of the individual 3-D position measurements made using a particular navigation system.
Sequential Receiver	A GPS receiver in which the number of satellite signals to be tracked exceeds the number of available hardware channels. Sequential receivers periodically reassign hardware channels to particular satellite signals in a predetermined sequence.
SNR	Signal-to-Noise Ratio, often expressed in decibels.
SPI	Serial Peripheral Interface, a synchronous serial channel.
SPS	Standard Positioning Service. A position service available to all GPS users on a continuous, worldwide basis with no direct charge. SPS uses the C/A code to provide a minimum dynamic and static positioning capability.
SRAM	Static Random Access Memory. A form of RAM that maintains its contents as long as power is supplied without the need for periodic refreshing. See DRAM.
SSP	Synchronous Serial Port
SV	Space Vehicle, the common abbreviation for a satellite.

TDOP	Time Dilution of Precision. A measure of how much the geometry of the satellites affects the time estimate computed from the satellite range measurements.
3-D Coverage	The number of hours-per-day with four or more satellites visible. Four visible satellites are required to determine a three-dimensional position. In the GPS constellation with full operational configuration (consisting of 21 primary satellites and at least 3 in-orbit spares), 3-D coverage is available at all times over the surface of the earth.
3-D Navigation	Navigation Mode in which altitude, horizontal position and the local time are determined from satellite range measurements.
TTFF	Time To First Fix. The actual time required by a GPS receiver to achieve a position solution after power is applied, or a reset is performed. This specification varies with the operating state of the receiver, the length of time since the last position fix, the location of the last fix, and the specific receiver design. See also Hot Start, Warm Start, and Cold Start.
2-D Coverage	The number of hours-per-day with only three satellites visible. Three visible satellites can be used to determine location if the GPS receiver is designed to accept an external altitude input (Altitude Hold).
2-D Navigation	Navigation Mode in which a fixed value of altitude is used for one or more position calculations while horizontal (2-D) position can vary freely based on satellite range measurements.
UART	Universal Asynchronous Receiver/Transmitter, adevice that produces an electrical signal and timing for transmission of data over a serial communications path, and circuitry for detection and capture of such data transmitted from another UART.
UDRE	User Differential Range Error. A one sigma estimate of the pseudorange measurement error due to ambient noise and residual multipath.
UERE	User Equivalent Range Error, an estimate of the pseudorange measurement error due to such system parameters as satellite clock and ephemeris error, and ionospheric model errors.
Update Rate	The GPS receiver specification that indicates the solution rate provided by the receiver when operating normally. Common update rates are once per second, twice per second, and 10 times per second.
UTC	Universal Coordinated Time. This time system uses the second defined true angular rotation of the Earth measured as if the Earth rotated about its Conventional Terrestrial Pole. However, UTC is only adjusted in increments of one second. The time zone of UTC is that of Greenwich Mean Time (GMT).
VCO	Voltage Controlled Oscillator
VDOP	Vertical Dilution of Precision. A measure of how much the geometry of the satellites affects the position estimate (computed from the satellite range measurements) in the vertical (perpendicular to the plane of the user) direction.
VSWR	Voltage Standing Wave Ratio
Warm Start	Start mode of the GPS receiver when current position, clock offset, and approximate GPS time are available in the receiver, but no current ephemeris is available. In a warm start, the receiver has sufficient information to predict which satellites are visible, but once these satellites are acquired, the receiver must learn their ephemerides by listening to their navigation messages.
WGS-84	World Geodetic System (1984). A mathematical ellipsoid designed to fit the shape of the entire Earth. It is often used as a reference on a worldwide basis, while other ellipsoids are used locally to provide a better fit to Earth in a local region. GPS uses the center of the WGS-84 ellipsoid as the center of the GPS ECEF reference frame, and the surface of the reference ellipsoid as the basis of latitude, longitude, and ellipsoidal altitudes.

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